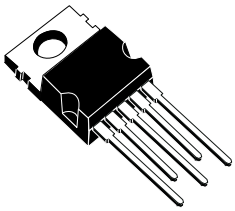
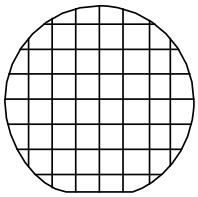
L9918

Datasheet

Alternator voltage regulator with LIN interface for 12 V applications



PENTAWATT In Line



Bare die

Features

- AEC-Q100 qualified
- Closed loop voltage control
- Regulated voltage with thermal compensation function
- High side excitation driver with internal freewheeling circuit
- Load response control (LRC) and Return LRC
- Self-start activation by phase signal
- Current limitation and overcurrent protection
- Thermal protection
- Physical Layer compliant with LIN 2.2A spec.
- Data Link Layer compliant with LIN 1.3, 2.1, 2.2 and 2.2A specification
- 13 sets of LIN frames selectable
- Configurable parameters (see NVM parameter table A1)
- Configurable for 5, 6, 7, 8 or 9 pole pair alternator
- Compliant to VDA LIN-Generator-Regulator specification
- Full ISO26262 compliant, ASIL-B systems ready
- Available as Bare die as well as in PENTAWATT In Line (TO220-5) package

Description

L9918 is an alternator voltage regulator equipped with LIN protocol interface.
The device is intended to be used in automotive application for 12 V systems.
The presence of NVM cells for device parameters programmability makes it suitable for a wide range of charging application.

Product status link
L9918

Product summary		
Order code	**Package**	**Packing**
L9918	PENTAWATT In Line (TO220-5)	Tube
L9918BDTR	Bare die	Tape&Reel

1 Functional description

The device is an alternator voltage regulator suited for 12 V system, able to communicate with ECU through LIN communication protocol.

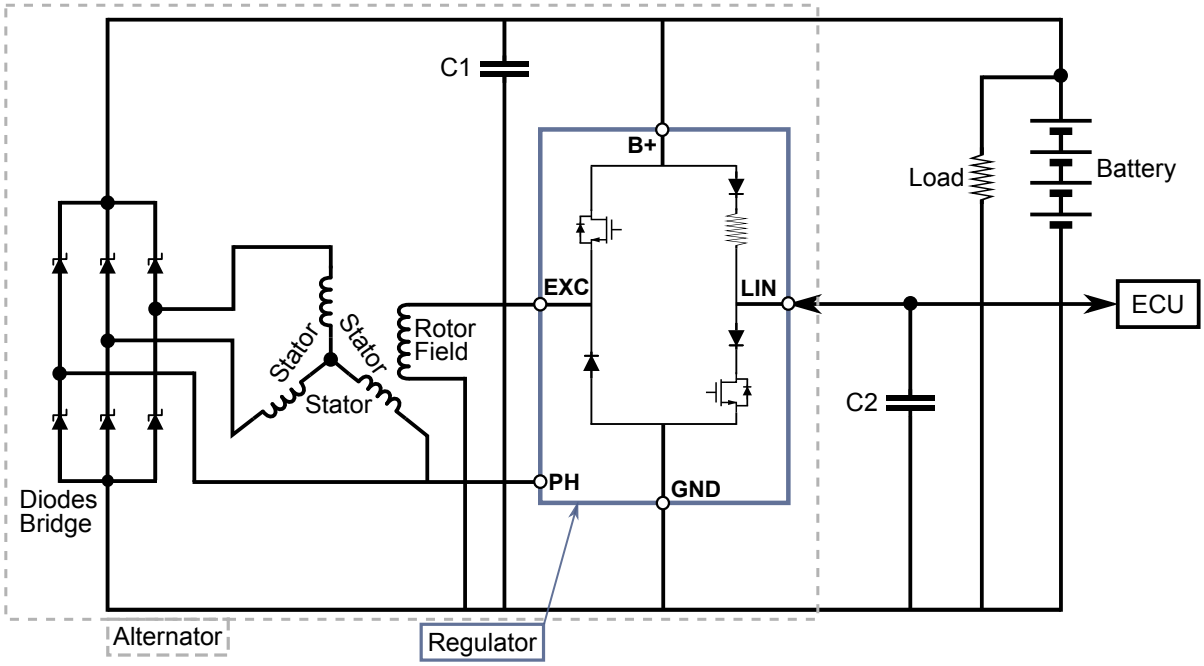
The device is housed into an alternator brush holder and it provides current to the excitation coil of the alternator (rotor) through a high side power MOSFET driver. The device is suitable for alternators with different poles pair number. An active freewheeling circuit is also integrated into the device.

Target function of the device is to modulate the rotor current in order to keep the voltage on car loads steady to a target value (set point), whatever the vehicle demand.

The set point target is typically commanded by the ECU and it is achieved using an internal voltage reference. Set point is communicated along with many others functional parameters during the regular device functioning.

Slew rate control in combination with external filtering of the interface lines helps to realize electromagnetic compatibility.

Figure 1. Simplified application diagram



1.1 External component required

The capacitors C1 (2.2 µF ceramic suggested) and C2 (220 pF suggested) to suppress radio frequency injection have to be connected as close as possible between the related pin and GND.

1.2 Pin description

Figure 2. **Pins connection diagram (top view)**

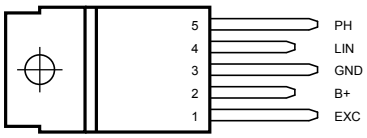


Table 1. **Pin description**

N°	PIN	Function
1	EXC	High side driver output to control the rotor current
2	B+	Device power supply and Battery voltage sensing
3	GND	Regulator ground
4	LIN	Communication terminal
5	PH	Phase sense input

1.2.1 EXC

This pin is connected to the excitation coil (rotor) of the alternator. The IC supplies a current to the rotor in order to control the output current of the alternator when car load or car speed varies. Device target is to maintain battery voltage at defined set point. Inside the device is also embedded a freewheeling circuit, needed to discharge the rotor current when the High Side power is turned OFF.

1.2.2 B+

The device is supplied by this pin. This voltage is also used as feedback voltage by the regulation loop.

1.2.3 GND

The device has one GND pin.

1.2.4 LIN

This LIN pin represents the single-wire bus transmitter and receiver. It is suited for automotive bus systems and is based on LIN protocol defined in LIN bus specification v1.3, v2.1, v2.2 and v2.2A.

1.2.5 PH

This pin is connected to one of the stator windings. Its input signal is used for rotor speed measurement, stator voltage monitoring as well as self-start detection. During the regulation, phase signal voltage level is continuously monitored. Phase regulation function is activated if phase amplitude is not addressing desired levels.

1.3 List of device features

The device is designed to satisfy the below features:

1.3.1 Standby current

When L9918 is in standby state, the average power consumption is very low over all temperatures. Current consumption can slightly increase while the device is evaluating wakeup sources: device perform a partial wake up in order to check if eventual signals on phase or LIN pin are valid wakeup events. However even during this partial wakeup, current consumption remains well below the wakeup state consumption.

1.3.2 Closed loop voltage control

L9918 regulates the voltage on car loads by closed loop control. Target voltage (set point) can be chosen by default (UR_DEF_REG NVM bits) or it can be sent by the Engine Control Unit (ECU) through LIN interface (VBSPLINRG).

1.3.3 Load response control (LRC)

The torque applied to the engine by the alternator is proportional to the alternator output current. If an electrical load is applied by vehicle harness, the torque applied to the engine can be too high to be sustained, especially if engine is running at low RPM. The LRC is intended to manage temporarily the alternator output current variation in order to limit torque demand variation.

On high rotational speeds, engines do not suffer from torque changes. For this reason load response is switched off for RPM > SPLRC,x such that any DC adjustment is executed immediately. The load response function will be active again if RPM < SPLRC,x condition is detected.

The LRC can be configured by ECU via LIN or it can adopt a default configuration (NVM programming).

To avoid permanent voltage adjustment with load response control (while RPM < SPLRC,x), even in case of small duty cycle variations, the regulator has a "blind-zone" range. If duty cycle variation falls within this range, LRC is not activated. Blind zone control can be programmed by TV_SPRUNG NVM bits.

The blind zone can be switched through LIN RX frame. This feature can be enabled or disabled by programming TV_SPRUNG_EN NVM bit. In case the feature is disabled (TV_SPRUNG_EN = 0) the regulator applies a programmed default value: blind zone can’t be changed via LIN and commands corresponding to BZ change into the RX frames are ignored.

1.3.4 Pre-excitation

Conditions for pre-excitation are defined in the internal state machine. In pre-excitation mode, the rotor is magnetized with a fixed duty cycle in order to produce an induced voltage as soon as the engine turns on.

Device behavior in pre-excitation is highly configurable. More detailed explanation on all the possible pre-excitation modes are provided in Section 4.2.3 Pre-excitation specific mode selection

1.3.5 Phase regulation

When the engine rotates and the device is regulating, the regulator requires a minimum voltage level on the stator coil signal (phase signal) in order to be ready for engine rotation speed measurement. Proper phase signal level is guaranteed by phase regulation function (Section 3.2.2 Phase regulation).

1.3.6 Low voltage function

When very low battery voltage is measured, current provided to the excitation coil is driven forcing excitation duty cycle at 100% until a minimum defined voltage is achieved (Section 2.2.4 UV/OV management).

1.3.7 Overvoltage safety function

L9918 implements an EXC switch off safety function in case of overvoltage detection (Section 2.2.4 UV/OV management).

1.3.8 Overvoltage function

Other than Overvoltage safety function, L9918 is equipped with a further overvoltage function, which allows filter time and threshold programmability (Section 2.2.4 UV/OV management).

1.3.9 Excitation current measurements

Device is equipped with a current sensor in order to measure the current flowing out from EXC pin (Section 4.2.6 Excitation current measurement).

1.3.10 Current limitation and overcurrent protection

Current limitation can be used to limit the EXC current. Current limitation activation threshold can be set by LIN or by specific NVM bits programming.

Overcurrent protection is an independent protection which command the shutdown of EXC power stage in case a maximum current threshold is overcame (Section 4.2.6 Excitation current measurement).

1.3.11 Temperature measurements

A temperature sensor monitors the junction temperature of the regulator. The tolerance is ±10 °C.

1.3.12 High temperature voltage limitation

L9918 implements a thermal compensation function in order to protect EXC field driver against high temperature (Section 2.2.3 Thermal compensation).

1.3.13 Self-start

The regulator can be activated even in case of failed or not activated LIN communication. After the self-start, the regulator performs as a multifunction stand-alone regulator with default parameters.

1.3.14 Non volatile memory (NVM)

L9918 contains an NVM memory with a high number of programmable bits. This allows users to apply many different configurations in order to address a wide range of applicative scenarios. NVM programming is operated by LIN communication through a specific “programming mode procedure” and it is typically done at the end of production line. NVM can be programmed 16 times at most.

1.3.15 Local interconnect network (LIN) interface

The regulator has a bidirectional serial data LIN interface to communicate with the Engine Control Unit (ECU). The Physical Layer is compliant with LIN 2.2A specification. The Data Link Layer is compliant with LIN 1.3, 2.1, 2.2 and 2.2A LIN specifications.

LIN configuration addresses following functions:

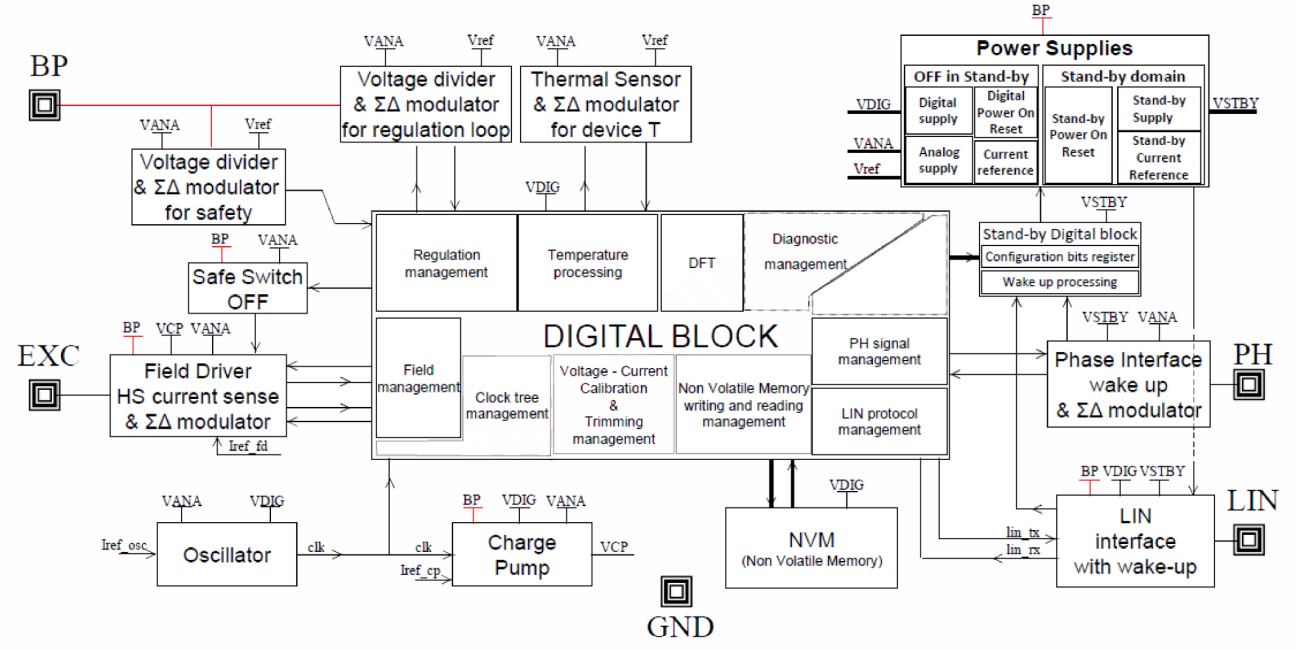
- Control of the set-point voltage regulation
- Control of LRC parameters (rise time, LRC disable speed, blind zone)
- Setting of the excitation current limitation
- Excitation duty cycle feedback
- Excitation current feedback
- High temperature feedback
- Diagnosis information feedback (LIN error and alternator failure detection)
- Alternator supplier code feedback
- Alternator class code feedback
- Chip supplier identification
- Chip identification

1.3.16 Compatibility with different alternator types

All the RPM speed values specified respect 5, 6, 7, 8 or 9 pole pair alternator definition.

1.4 Internal block diagram

Figure 3. **Simplified block diagram**



1.4.1 Power supplies

Power Supplies block contains two sub-blocks: the first is always working, even when device is in stand-by state (Stand-by domain); the latter works just when the device is in active states (OFF in stand-by).

The first sub-block supplies Phase and LIN interfaces (needed for the wake up function) and the Stand-by digital block.

The second sub-block provides the analog and digital supplies to the whole device when PH or LIN pins are fed with a valid signal. It even provides voltage references for all the sigma-delta converters and provides currents reference as well. This sub-block is not supplied in stand-by state.

1.4.2 Phase interface

The task of this block is to detect activity on phase pin and verify if the phase signal voltage levels are correct. The circuitry in charge of phase activity detection is always supplied in stand-by.

1.4.3 LIN interface

The block controls the LIN bus transmission and reception. The circuitry in charge of LIN bus activity detection is supplied in stand-by as well.

1.4.4 Stand-by digital block

The Stand-by digital block manages the information coming from interfaces and, taking into account NVM configuration data, eventually generates a wake-up signal.

1.4.5 Voltage divider & ΣΔ modulator for regulation

The stage has a resistive divider connected to battery and provides the correct signal voltage range to the internal converter stage. The stage feeds into the digital block a bit-stream converted in a digital code with a proper low pass filter. The code is managed in the digital block to act the regulation.

1.4.6 Voltage divider & ΣΔ modulator for overvoltage/undervoltage

The stage has a resistive divider connected to battery (different and independent of the previous stage) and provides the correct signal voltage range to the internal data converter. The stage feeds into the digital block a bit-stream converted in a digital code with a proper low pass filter. The code is managed in the digital block to implement the overvoltage and under-voltage detections.

1.4.7 Thermal sensor

Thermal sensor provides to the digital block the device temperature. The block embeds a thermal sensor and a sigma-delta converter whose bit-stream is converted in a digital code.

1.4.8 Oscillator

The block provides the clock reference for the digital function and the Charge Pump block. The frequency value is 16MHz ± 5%.

1.4.9 Excitation driver

The block embeds a power N-channel MOS inserted between B+ and EXC pins and a circuitry that is able to drive it. A freewheeling circuit is inserted between EXC and GND pins, located across the excitation coil for energy recirculation purpose. The protection against short circuit on EXC pin is also implemented. If a short circuit is detected the excitation current is turned off and the subsequent turn-on attempt is retried at every excitation period.

A current measurement block provides the excitation current value flowing in the high-side power MOS. In order to reach the requested accuracy, a dedicated thermal sensor is located close to the current measurement block. Power MOS temperature is used to calibrate the current measure.

1.4.10 Safety switch OFF

Safety Switch OFF is a separate block featured for safety reason. It must switch the field driver power MOS gate off when a battery overvoltage condition is detected.

1.4.11 Charge pump

Charge pump is mandatory to supply correctly the excitation power MOS gate.

1.4.12 Non volatile memory (NVM)

The NVM allows to set all configurable device parameters. Please refer to default mode parameter table (see Section A.1).

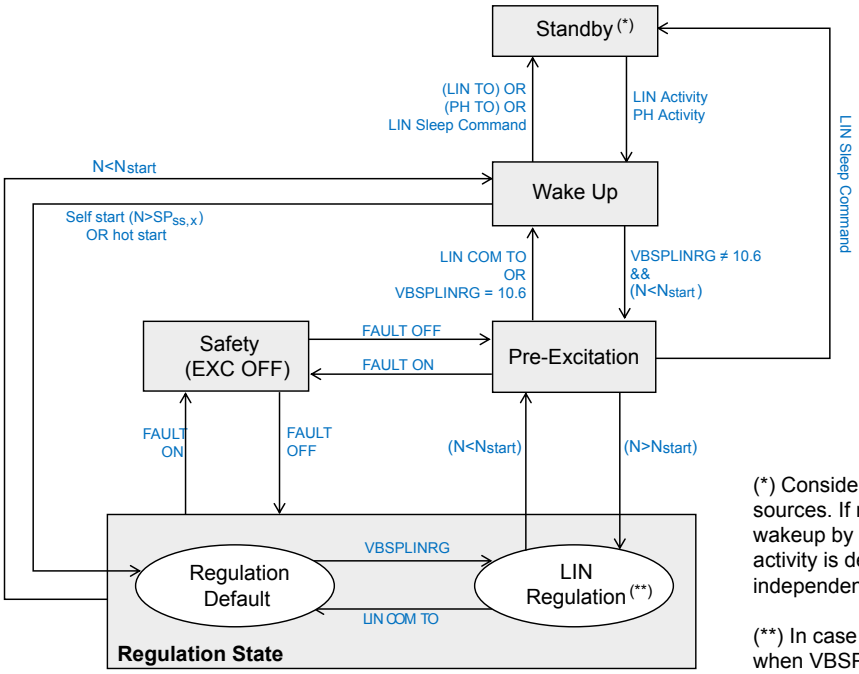
1.4.13 Digital block

All device functions are managed by the digital block. The state diagram is shown in the next chapter.

1.5 State diagram

The following figure describes L9918 state machine.

Figure 4. **L9918 finite state machine diagram**



(*) Considered timeout depends on the wakeup sources. If no LIN activity is detected (device wakeup by phase) device consider PH TO. If LIN activity is detected, adopted timeout is LIN TO, independently of the wakeup event.

(**) In case REG_AUS = 0x1, EXC is disabled when VBSPLINRG = 10.6.

1.5.1 Standby

Device conditions to enter in stand-by mode:

- LIN time-out or phase time-out;
- LIN sleep command.

Device considers two different timeouts to go back to standby from wake up: LIN timeout and phase timeout.

LIN timeout means: no activity on LIN bus during specified time (see t_{LIN_to} parameter).

Phase timeout means: no activity on phase signal during a specified time (see t_{PH_to} parameter).

Standby entrance from Wake Up state can be done accordingly to one of the two timeouts. In case no LIN activity is detected (wake up by phase), device goes in standby if no more PH activity occurs for longer than t_{PH_to}.

If LIN activity is detected, device transition from Wake Up to Standby uses tLIN_to independently of the wake up source.

The standby mode can even be forced by ECU sending LIN sleep command.

In stand-by state the device has:

- No excitation. Duty cycle (DC) on EXC pin is equal to zero.
- Current consumption aligned to $IB_{stbyL80}$, $IB_{stbyH80}$, according to the internal temperature.

In this state the device needs a small amount of quiescent current to supply logic, phase detector and LIN receiver only.

When device is supplied after a shutdown, as soon as the voltage reaches VB_{POR} threshold, the digital block in charge of evaluate input coming from PH and LIN pins is initialized. For this reason only B+ levels higher than VB_{POR} can ensure device wakeup functionalities.

1.5.2 Wake-up

This state is reached from Standby if at least one of the following wake up sources occur:

- Activity is detected on LIN bus (LIN wakeup event selected by LIN_WAKEUP_PATTERN NVM bits, accordingly to LIN specification document).
- Activity on PH pin is detected ($VP_{StartTh}$).

Wake up state can also be accessed from Pre-excitation state in case no valid communication is provided for more than LIN COM timeout (t_{LIN_COM}) or in case VBSPLINRG = 10.6 is received.

Device remains in wake up state as long as at least one of the listed wake up source is present. If wake up sources are no longer detected, the device goes back in stand-by with a proper time-out.

Every time the device enters the wake up state from standby state, an initialization procedure consisting in an NVM download procedure is triggered. Every volatile data so far acquired (i.e. setup commanded through LIN Rx frames) are lost.

In wake up state:

- All the blocks are ON, the current consumption is higher than standby current consumption.
- The duty cycle on EXC pin is equal to zero.
- The phase sensitivity is $VP_{StartTh}$ (peak to peak).

In case of cranking event, due to low battery voltage value, LIN protocol could not be working. LIN timeout can occur and the parameters sent by LIN protocol will be lost.

One particular behavior related to Wake Up state is the behavior occurring when device detects activity (i.e. TX frames or RX frames with unrecognized ID or checksum) on LIN bus. Once this activity is detected, device doesn't move toward regulation state even if valid PH is present. It keep EXC OFF, waiting for a valid set point command.

Phase regulation is active into Wake-up state. It is performed just in case phase rotation greater than N_{start}.

1.5.3 Pre-excitation

The pre-excitation state is reached as soon as VBSPLINRG differs from 10.6 V and the engine rotation is lower than N_{start}.

The purpose of pre-excitation is to increase the alternator magnetization in order to guarantee proper conditions for PH signal measurement in case the engine start to rotate. The pre-excitation is done driving the alternator rotor with a PWM signal that has fixed frequency ($fF_{SWpreexc}$) and fixed duty cycle (25 %).

If the battery voltage is higher than the maximum set-point value selectable by LIN protocol (V_{B+_LIM}) the duty cycle is reduced to 8 % or to 0 %, depending on NVM bit SST_ULIM_TV0_EN.

In pre-excitation state:

- LRC function is disabled.
- Phase regulation is disabled.
- Current limitation control by LIN disabled except for specific pre-excitation mode (described below).
- Default EXC current limitation is activated by dedicated NVM bits (IMAX_VE and IMAX_VE_VAL).
- Safety functions are enabled.

Device is even featured with a specific pre-excitation mode, selectable by SV_FORD_EN NVM bit. When this is enabled, EXC signal behavior depends on B+ value respect to the set point (VBSPLINRG) and on LIN frame data carried by the LIN RX frame.

More detailed explanations and examples on special mode can be found in Section 4.2.3 Pre-excitation specific mode selection.

1.5.4 Regulation mode

1.5.4.1 LIN regulation mode

This state can be reached: from pre-excitation state when alternator rotation is higher than Nstart; from Regulation default state when valid set-point (VBSPLINRG > 10.6 V) is provided.

In particular, more detailed explanations must be dedicated to the last of these cases (LIN Regulation entered from Regulation Default). If the Regulation Default state persists for more than LIN TO, two frames are needed to enter the LIN Regulation mode: the first one to wake up the LIN block, the second one to communicate LIN regulation data. On the other hand, if Default Regulation persist for less than LIN TO, the device is ready to receipt LIN regulation information by a single LIN RX frame. In such case LIN Regulation mode can be entered sending just one RX frame.

In this state the device modulates the EXC output current in order to set the battery line voltage to the LIN set point (VBSPLINRG).

In LIN regulation mode state:

- LRC function enabled accordingly to LIN communication.
- Phase regulation enabled.

- Current limitation enabled accordingly to current limitation thresholds provided by LIN or by NVM registers contents (the lower between the two current limitation thresholds is adopted).
- Safety functions active.
- Thermal compensation enabled.
- Low voltage function.

1.5.5 Regulation default

This mode is equivalent to the LIN regulation mode except that, being without LIN communication, NVM default regulation parameters (VBSPDEF, TFLRCup, TFLRCdw, SPLRC) are used for regulation.

Regulation default can be entered from wake-up state when phase rotation is greater than SPSS (N_NOTSTART NVM register). Phase amplitude required to enter regulation default depends on KLV_AC_ADAP_MIN_NOT, KLV_AC_ADAP_MIN and ACADAPMIN_MODE NVM registers.

Regulation default can be entered from LIN regulation state in case no valid frame is provided for a time longer than tLIN_COM, adopted set point changes from VBSPLINRG to VBSPDEF.

Set point transition to default VBSPDEF is performed with a ramp of VBSP_LDslope and excitation current limitation moves to IFELD_MAXB or I_MAX with a ramp of $IF_{LIM\_LDslope}$.

If LIN communication resumes, regulation voltage and current limitation target change immediately, accordingly to the received RX frame data.

In regulation default state:

- LRC function enabled accordingly with NVM selection.
- Phase regulation enabled.
- Current limitation set to IFELD_MAXB and I_MAX.
- Safety function enabled.
- Thermal compensation enabled.
- Low voltage function.

1.5.6 Safety

Safety state is an excitation OFF state which is entered as soon as a safety protection mechanism is activated while device is into pre-excitation or regulation state.

Here below a list of the safety mechanisms implemented by L9918:

1.5.6.1 Current protection

In all the states where the excitation power MOS is active, overcurrent protection function is working. As soon as the IF_{OCP} threshold is reached the power is switched OFF.

1.5.6.2 Thermal protection

In case T_J reaches the $T_{sd,x}$ threshold (selectable by NVM bits THERMAL_TH_SEL), EXC power MOS is switched OFF till the T_J temperature decrease below $T_{sd,x}$ - T_{sdhy}.

1.5.6.3 Overvoltage safety protection

In case of B+ > $VB_{OV\_safetyL}$ for more than $T_{OVflt\_safetyL}$ or B+ > $VB_{OV\_safetyH}$ for more than $T_{OVflt\_safetyH}$, EXC power MOS is switched OFF till B+ returns at a value lower than $VB_{OV\_safetyL}$ for more than $T_{OVflt\_safetyL}$ time.

1.6 Product characteristics

1.6.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit
VB_{LD}	Transient supply voltage (load dump) t < 400 ms				Vcl	V
I_{Bond}	DC pin current on EXC, B+, GND (bonding limitation)				15	A
ESD_{HBM}	ESD HBM (All pins vs.GND) R=1.5kΩ, C=100pF, RT=25°C		-8		8	kV
ESD_{CDM}	ESD CDM on EXC and PH pins		-750		750	V
ESD_{CDM}	ESD CDM on B+ and LIN pins		-500		500	V

1.6.2 Internal clamping structure

Table 3. Internal clamping structure

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit
Vcl	Internal central clamp voltage	B+ current injected I=20mA	58		64	V
Vcl_LIN	Dedicated Clamp to LIN pin	Current injected in LIN pin I=20mA	40		-	V

1.6.3 PIN number - absolute maximum ratings - operative range

Table 4. PIN number - absolute maximum ratings - operative range

n.	Pin	ABS max rating		operative range		Unit
		Min.	Max.	Min.	Max.	
1	EXC	- 2	B+	- 1.6	B+	V
2	B +	-0.3(1)-	Vcl(3)	6	18	V
3	GND	-	-	-	-	
4	LIN	-27(2),(3)	Vcl_LIN	- 3	18	V
5	PH	-27(2)	Vcl	- 3	18	V

1. *3.2 V, transient 5 s.*
2. *Value at cold temperature: -25 V.*
3. *LIN and B+ AMR not valid at the same time.*

1.6.4 Thermal data

Table 5. Thermal data

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit
Rth_j-case	Thermal resistance junction-to-case	Related to TO220			2	°C/W

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit
Tsd,1	Thermal shutdown threshold	Temperature to disable EXC driver for chip protection (set by THERMAL_TH_SEL)	170	180	190	°C
Tsd,2			165	175	185	°C
Tsd,3			175	185	195	°C
Tsd,4			180	190	200	°C
Tsdhy	Thermal shut-down hysteresis	EXC from OFF STATE (due to thermal shutdown) to ON STATE	2	6	10	°C
Temp_R	Tj for full functional and full spec		-40		150	°C
Temp_F	Tj for full functional with parameters deviation		150		190	°C
Temp_SRctrl	Current SR disable temperature	Tj over which EXC current slew rate control is disabled (SR_HT_DIS)	125	135	145	°C
Temp_SRctrl_hist	Temp_SRctrl hysteresis	Hysteresis from “disabled” state (entered because Tj>Temp_SRctrl) to “enabled” state		6		°C
Tstg, Tcase	Storage and case temperature range		-40		150	°C

2 Power supply and battery voltage sensing - B+ pin

Unless otherwise specified, all the electrical characteristics provided in this chapter refers to T_j between -40 °C and 150 °C.

2.1 B+ electrical characteristic

Table 6. B+ electrical characteristic

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit
VB_{OpVR}	Operating Voltage Range		6		18	V
VB_{deepLV}	Deep low Voltage Range	parameter degradation, not reset (according to ISO16750 - cranking)	3		6	V
$IB_{stbyL80}$	Stand-by current consumption lower 80 °C	VB+ = 12.5 V; VPH = 0; VLIN = 12.5 V; T < 80 °C	1		50	µA
$IB_{stbyH80}$	Stand-by current consumption higher 80 °C	VB+ = 12.5 V; VPH = 0; VLIN = 12.5 V; T > 80 °C	1		100	µA
IB_{active}	Current consumption out of stand-by	VB+ = 12.5 V; No current load on EXC and LIN		18	30	mA
$VB_{SPLINRG}$	Set-Point Voltage Range for LIN communication	VPH = 10 Vpp square wave at 500 Hz; valid LIN communication; @ Tj = 30 °C	10.6		16	V
VB_{SPDEF}	Default Set_Point Voltage Range (no LIN communication) (NVM UR_DEF_REG)	VPH = 10 Vpp square wave at 500 Hz; no LIN communication; @ Tj = 30° C	10.6		16	V
VB_{SP_tol30}	Set_Point voltage tolerance Tj = 30 °C	VPH = 10 Vpp square wave at 500 Hz; with/without LIN communication (please refer to Figure 5)	-100	0	+100	mV
$VB_{SP\_tolTrange}$	Set_Point Voltage Tolerance-40 °C < Tj < 150° C	VPH = 10 Vpp square wave at 500 Hz; with/without LIN communication ((please refer to Figure 5)	-150	0	+150	mV
ΔVB_{load}	Regulated Voltage variation with the load	Difference between regulated voltage when EXC duty cycle is 10 % and regulated voltage when EXC duty cycle is 90 %			I_ANT/P_ANT	V
ΔVB_{speed}(1)	Regulated Voltage variation with the speed	Difference between regulated voltage when Ialt = 10 A; 2000rpm < Alt speed < 18000rpm	-50		100	mV
$VB_{SP\_LDslope}$	Voltage Slope to address default Set Point starting from LIN Set Point		0.18	0.2	0.22	V/s

1. *Not subject to production test, specified by design (alternator dependent).*

The maximum tolerated ripple value on B+ is ± 6 V whatever speed and load. In case voltage ripple on battery line exceeds this limit, declared tolerance cannot be guaranteed,

Figure 5. **Set point voltage tolerance versus temperature: example with 14V set point (VBSPLINRG or VBSPDEF).**

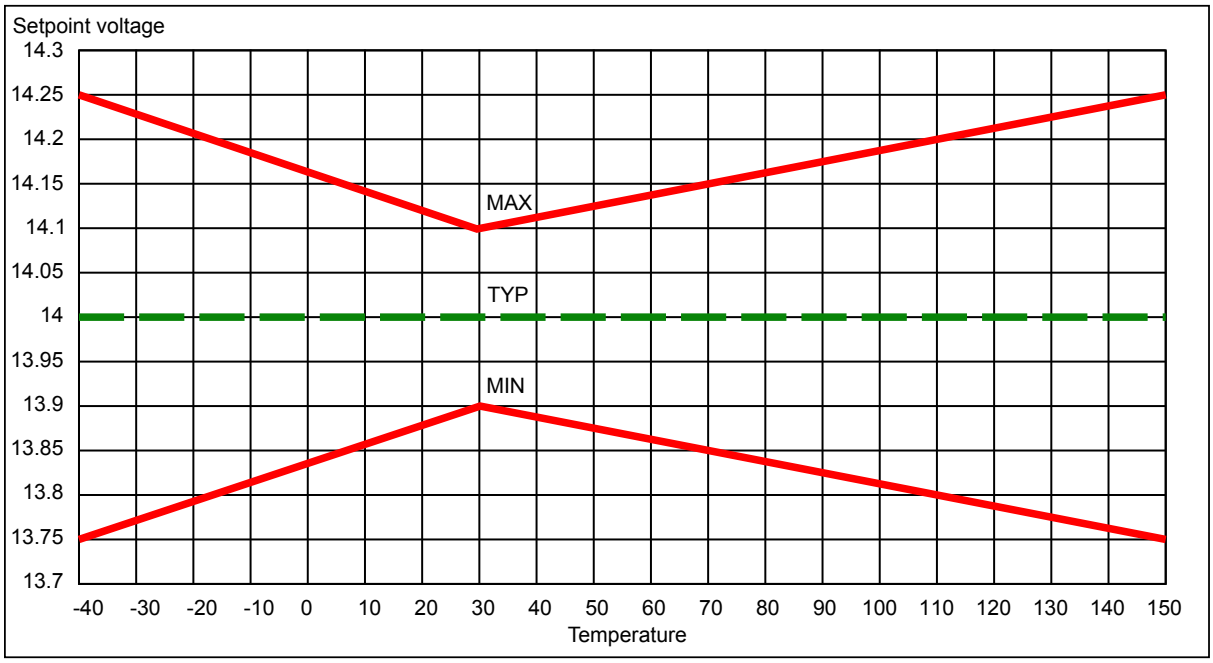


Table 7. **Over and under voltage parameters**

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit
VB_{OV1}	Over-voltage function threshold (U_FELD_AUS)		16.0	16.5	17	V
VB_{OV2}			16.5	17	17.5	V
VB_{OV3}			17	17.5	18	V
VB_{OV4}			17.5	18	18.5	V
$VB_{OVft,1}$	Bidirectional Over-voltage filter time (U_FELD_AUS_TIME)			520		µs
$VB_{OVft,2}$				780		µs
$VB_{OVft,3}$				1040		µs
$VB_{OVft,4}$				0		µs
$VB_{OV\_safetyL}$	Over-voltage for safety low threshold		16.5	17	17.5	V
$VB_{OV\_safetyH}$	Over-voltage for safety high threshold		17.5	18	18.5	V
$T_{OVflt\_safetyL}$	Over-voltage filter time for safety low threshold			1		s
$T_{OVflt\_safetyH}$	Over-voltage filter time for safety high threshold		0.405		0.482	s
$V_{LOW,1}$	Low-Voltage threshold (U_FELD_EIN)		8.5	8.75	9	V
$V_{LOW,2}$			9	9.25	9.5	V
$V_{LOW,3}$			9.5	9.75	10	V
$V_{LOW,4}$			9.75	10	10.25	V
$V_{LOW,5}$			10	10.25	10.5	V
$V_{LOW,6}$			10.25	10.5	10.75	V

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit
$V_{LOW,7}$	Low-Voltage threshold (U_FELD_EIN)		10.75	11	11.25	V
$V_{LOW,8}$		VLOW = 9.9 V + 0.388 * (VSET - 10.6 V)		PSA		V
V_{B+_LIM}	Set point limit threshold			16		V
$VB_{LVft,1}$	Bidirectional Low-voltage filter time (U_FELD_EIN_TIME)			529		µs
$VB_{LVft,2}$				780		µs
$VB_{LVft,3}$				1040		µs
$VB_{LVft,4}$				1200		µs
VB_{POR}	Power On Reset when is elapsed at least td time		2.7		3	V
td	Max battery interruption time				80	µs
t1	Minimum time between two battery interruptions		1			ms

2.2 B+ characteristics

2.2.1 Set point value correction

It is possible for the customer at end of line to perform a set-point voltage value correction by dedicated NVM bits (UR_OFFSET). The set-point voltage value can be adjusted from - 200 mV to 150 mV with steps of 50 mV. Such voltage correction applies both to default set point (VB_{SPDEF}) and LIN set point ($VB_{SPLINRG}$).

2.2.2 Voltage regulation loop

Regulation loop circuit is composed by two main blocks: direct (or proportional) control block and feedback (or deviation) control block.

Direct or proportional control applies an EXC DC correction which directly depends on the calculated error (which is obtained as B+ - VBSPLINRG/VBSPDEF).

Proportional control can be selected by P_ANT NVM bits. Small values of P_ANT correspond to a high regulation sensitivity.

Figure 6 (P_ANT regulation) reports the output voltage (B+) variation depending in the EXC DC in case only proportional regulation is used.

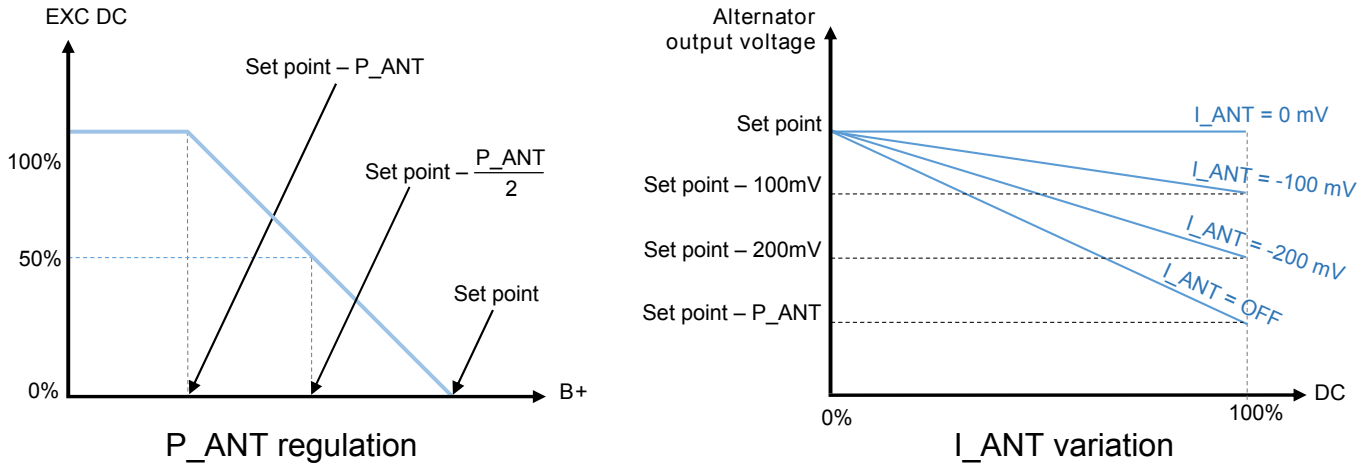
Feedback (or deviation) control is a set point correction which depends on EXC DC.

Such correction shall be used in order to compensate eventual voltage drop occurring between car battery and car loads and regulator B+.

Feedback control options can be selected by I_ANT NVM bits. High values of I_ANT correspond to a high offset on the adopted set point. I_ANT offset is applied after a filter time selectable by I_FILT NVM bits.

Figure 6 (I_ANT variation) reports the dependency between EXC DC and B+ for various I_ANT settings.

Figure 6. **Dependency between B+ and EXC duty cycle in case of P_ANT regulation and I_ANT variation**



2.2.3 Thermal compensation

Thermal compensation function is a protection function whose aim is to reduce current flowing out from EXC pin when a too high junction temperature is sensed.

This function operates as reported in Figure 6. Adopted set point is gradually reduced in case measured Tj is greater than thermal compensation threshold T_{HT}.

T_{HT} threshold can be programmed by HT_KN NVM bits. In some LIN configuration an offset can be added to HT_KN (Section A.7 Voltage limitation for high temperatures), so that T_{HT} = HT_KN + LIN offset. Maximum value of the adopted T_{HT} value is furthermore clamped to HT_KN_MAX. This means that the operative T_{HT} value is chosen as the minimum between HT_KN_MAX and HT_KN + LIN offset.

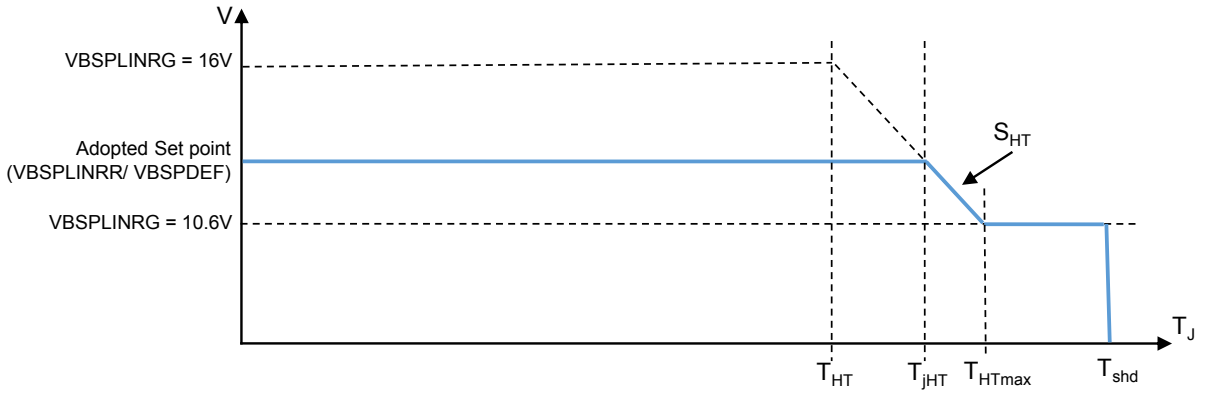
Once thermal compensation function is active, maximum set point is reduced accordingly to S_{HT} slope [mV/C] which can be set by NVM register HTK_SLOPE. As Tj increase, the maximum adopted set point decreases.

Thermal compensation dynamic behaviour is influenced by NVM bits G_HT, by which is possible to select the desired set point variation time gradient.

A further option related to thermal compensation is selectable by NVM bit HTKMAX_EN. This bit enables a temperature threshold T_{HTmax} over which adopted setpoint is forced to 10.6 V. T_{HTmax} value is fixed to 176 °C.

In case the NVM bit ANZ_HT_EN = 0x1, F_T LIN flag is set to "1" as soon as the set point currently adopted is modified by thermal compensation.

Figure 7. **Thermal compensation**



2.2.4 UV/OV management

Overvoltage Safety function

For safety reason this function is implemented with independent circuitry respect to the Overvoltage function. Safety Overvoltage function switches OFF the excitation driver through a dedicated path in order to guarantee that the function is always properly operated.

Safety Overvoltage detection is referred to $VB_{OV\_safetyL,H}$ thresholds and it is applied after $T_{OVflt\_safetyL,H}$ filter time. Such time is used even to calculate the elapsing of Safety Overvoltage condition.

Whenever the device exits the stand-by state, the safety overvoltage detection is disabled for 2 minutes in order to guarantee the jump start functionality. Jump start inhibits OV safety functions but it doesn't inhibit OV function (related to U_FELD_AUS).

Overvoltage function:

Overvoltage beyond $VB_{OV,x}$ due to, i.e., switching off of electrical loads, leads to switching off the output stage, if present for longer than $VB_{OVft,x}$. To avoid complete de-energizing of the alternator, phase regulation function can be enabled during Overvoltage function (LD_NR_DIS NVM bit). When Overvoltage condition is over, regulation re-adjusts to the set value. The function is active in "Regulation" state only (please refer to Section 1.5 State diagram).

The level for Overvoltage function activation and the correspondent filter time are defined by U_FELD_AUS and U_FELD_AUS_TIME NVM bits.

Low voltage function:

In case of high electrical load switching-on, especially with defect or missing battery, the voltage of the power net can drop to low values. If the voltage falls under the minimum operating voltage, the alternator can de-energize.

The duration of the voltage drop is minimized with the activation of the power stage as soon as, for longer than $VB_{LVft,x}$ voltage drops below V_{LOW}. While the low voltage function is active, EXC current limitation set via LIN is disabled. When B+ rises again over V_{LOW}, an active load response will smoothly resume its operation. The (V_{LOW}) threshold value is selectable by NVM bits (U_FELD_EIN).

Low voltage function can be enabled or disabled programming PRIORITY_CH_DIS bit.

Low voltage function can be implemented by two different strategies selectable by PRCH_LRC_EN NVM bit.

In case PRCH_LRC_EN = 0x0, PRIORITY_CH_DIS=0x0 is selected, 100 % EXC duty cycle is applied until B+ value returns greater than V_{LOW}. Once this threshold is crossed, adopted EXC duty cycle is the one calculated by the voltage regulation loop.

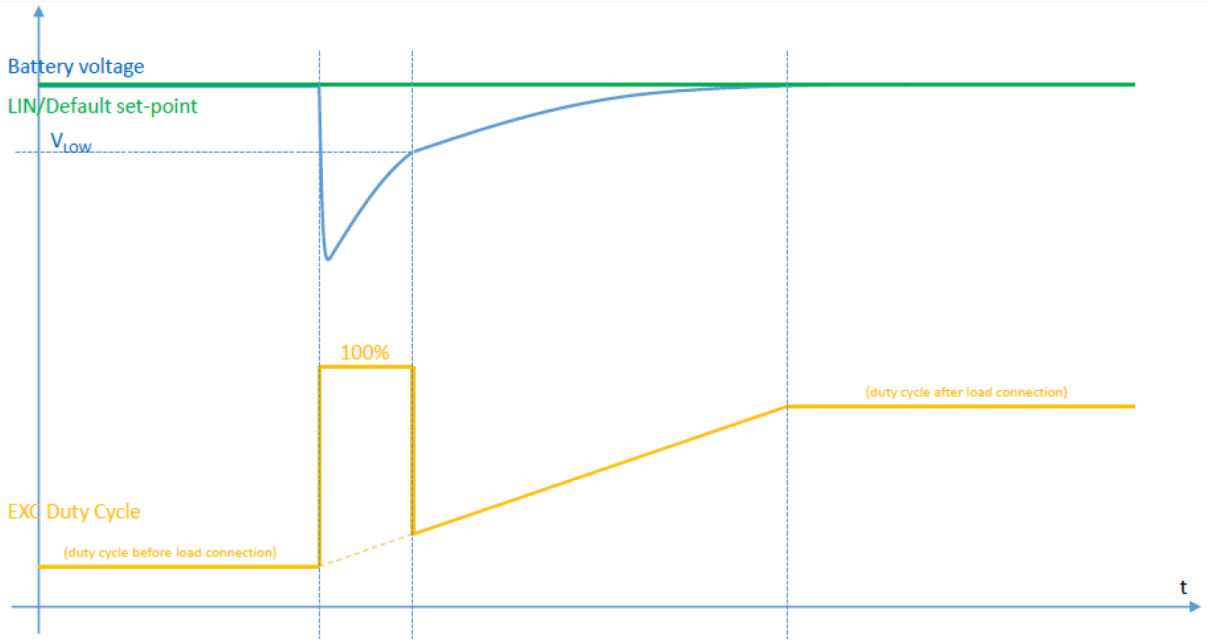
For PRCH_LRC_EN = 0x1, PRIORITY_CH_DIS = 0x0, Low voltage function behaviour is depicted in Figure 7: when low voltage function is activated, 100 % EXC DC is applied until B+ crosses VLOW threshold. For B+ values greater than V_{LOW}, a fixed DC increasing slope (0.78 % every EXC period) is applied.

In case, PRCH_LRC_EN = 0x0, PRIORITY_CH_DIS = 0x1, low voltage function is deactivated and EXC duty cycle is the one calculated by the voltage regulation loop.

For PRCH_LRC_EN = 0x1, PRIORITY_CH_DIS = 0x1, low voltage function is deactivated and EXC duty cycle for both B+ lower than VLOW and above V_{LOW} , a fixed DC increasing slope (0.78 % every EXC period) is applied.

When detected, the electrical fault F_E is set to 1 if the "F-EL on Low Voltage" bit (ANZ_LV_EN) of NVM bit has been set to 1.

Figure 8. **Low voltage function behavior**



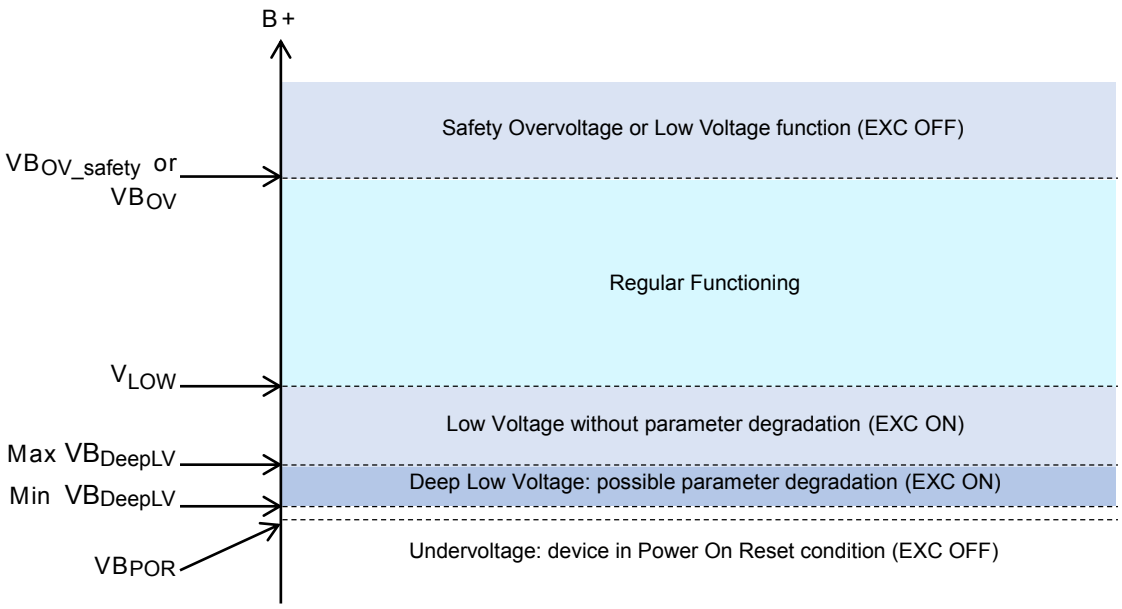
Behaviour in case of under voltage detection:

When the battery voltage is lower than POR threshold (VB_{POR}) and td time is elapsed, the device enters in standby condition showing a low power consumption.
The device can sustain micro-interruption in battery line without having a logic reset.

Deep Low Voltage range:

When B+ falls in deep low voltage range (VB_{deepLV}) the device isn't under reset and regulation loop computation is functioning, with possible degradation of parameters. However EXC operation is reduced.

Figure 9. **Battery voltage range**



The picture reports main voltage operation ranges.

Behaviour in case of Battery disconnection:

In case of vehicle battery disconnection, regulation loop parameters can be modified by LIN in order to compensate the sudden change of the load electrical conditions.

This feature can be enabled by REG_PARA_EN NVM bit.

3 Phase sense input - PH pin

Unless otherwise specified, all the electrical characteristics provided in this chapter refers to T_j between -40 °C and 150 °C.

3.1 PH electrical characteristic

Table 8. PH electrical characteristic

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit
$VP_{StartTh}$	Minimum peak to peak voltage on the phase to wake up the regulator	Phase average voltage is 0 V	150	200	500	mV
$VP_{HThREG,1}$	Phase regulation high threshold used when device is into regulation state. (KLV_NRSW)			4.0		V
$VP_{HThREG,2}$				5.5		V
$VP_{HThREG,3}$				7.0		V
$VP_{HThREG,4}$				7.7		V
$VP_{HThREG,5}$				9.0		V
$VP_{HThREG,6}$				9.5		V
$VP_{HThREG,7}$				10.2		V
$VP_{HThREG,8}$				10.4		V
$VP_{HThREG,9}$				10.6		V
$VP_{HThREG,10}$				10.8		V
$VP_{HThREG,11}$				11.0		V
$VP_{HThREG,12}$				11.2		V
$VP_{HThREG,13}$				11.4		V
$VP_{HThREG,14}$				11.6		V
$VP_{HThREG,15}$				11.8		V
$VP_{HThREG,16}$				12.0		V
$VP_{HThSS,1}$	Phase regulation high threshold used when device is out from regulation state. (KLV_USSW)			6.0		V
$VP_{HThSS,2}$				6.2		V
$VP_{HThSS,3}$				6.4		V
$VP_{HThSS,4}$				6.6		V
$VP_{HThSS,5}$				6.8		V
$VP_{HThSS,6}$				7.0		V
$VP_{HThSS,7}$				7.2		V
$VP_{HThSS,8}$				7.4		V
$VP_{HThSS,9}$				7.6		V
$VP_{HThSS,10}$				7.8		V
$VP_{HThSS,11}$				8.0		V
$VP_{HThSS,12}$				8.2		V

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit
$VP_{HThSS,13}$	Phase regulation high threshold used when device is out from regulation state. (KLV_USSW)			8.4		V
$VP_{HThSS,14}$				8.6		V
$VP_{HThSS,15}$				8.8		V
$VP_{HThSS,16}$				9.0		V
$VP_{LTh,1}$	Phase regulation low threshold(KLV_LOWSW)			1.8		V
$VP_{LTh,2}$				2		V
VP_{adth_HT}	Adaptive PH threshold mean value			3		V
RP_{pd}	Pull-down resistor (VPH=6V and VB+ = 14.5)			72		kΩ
TP_{SR}	Spike rejection time		70	125	180	µs
N_{Start}	Alternator speed threshold to enter in regulation mode		514	570	626	rpm
$SP_{SS,x}$	Self-start Alternator speed Threshold (no valid LIN communication)(selectable by N_NOTSTART NVM bit)		N_NOTSTART (+/- 10%)			rpm
$SP_{LRC,1}$	LRC disable speed Threshold (no valid LIN communication)(selectable by LRDN_DEF NVM bits)		2700	3000	3300	rpm
$SP_{LRC,2}$			3600	4000	4400	
$SP_{LRC,3}$			4320	4800	5280	
$SP_{LRC,4}$			5400	6000	6600	
$T_{LRC\_tvfilt,1}$	Filter time constant of duty cycle (LR_TVFILTTIME)	Tested for PWM_FREQ = 400Hz		20		ms
$T_{LRC\_tvfilt,2}$				40		ms
$T_{LRC\_tvfilt,3}$				60		ms
$T_{LRC\_tvfilt,4}$				80		ms
$T_{LRC\_tvfilt,5}$				100		ms
$T_{LRC\_tvfilt,6}$				120		ms
$T_{LRC\_tvfilt,7}$				140		ms
$T_{LRC\_tvfilt,8}$				160		ms
$T_{LRC\_tvfilt,9}$				180		ms
$T_{LRC\_tvfilt,10}$				200		ms
$T_{LRC\_tvfilt,11}$				220		ms
$T_{LRC\_tvfilt,12}$				240		ms
$T_{LRC\_tvfilt,13}$				2.5		ms
$T_{LRC\_tvfilt,14}$				5		ms
$T_{LRC\_tvfilt,15}$				7.5		ms
$T_{LRC\_tvfilt,16}$				10		ms
t_{PH_to}	Max windows time to detect 4 phase periods		114	128	142	ms
V_{adth_mid}	Adaptive PH thresholds mean value			3		V

3.2 PH characteristics

3.2.1 Alternator pole pairs

The selection of the correct alternator pole pairs is needed in order to make the device able to deduce the engine rotation speed (RPM) from PH signal frequency (Hz):

$$Rotation[RPM] = \frac{PH_{freq}[Hz]*60}{N_{pp}} \quad (1)$$

Where Npp is the alternator pole pairs number.

Possible selections for Npp are: 5, 6, 7, 8 and 9 (POLZ NVM bits).

3.2.2 Phase regulation

When the engine rotates and there is no alternator output current, the regulator has to recover a minimum voltage on the stator coil in order to be ready for alternator rotation speed measurement.

When device detect that phase recovery is needed, EXC DC is no more driven by regulation loop logic but it starts to be driven by Phase regulation function.

Starting of phase regulation function: the regulator monitors the phase voltage signal and checks if it oscillates between two selected thresholds:

- High threshold is selected depending on device state: if device is into Regulation state, high PH regulation adopted threshold is $VP_{HThREG,x}$, otherwise adopted threshold is $VP_{HThSS,x}$. These two thresholds can be programmed through KLV_NRSW and KLV_USSW NVM bits, respectively.
- Low threshold value is VP_{LTh}. Its value can be chosen between 1.8 and 2 V (KLV_LOWSW).VP_{LTh} can be either taken into account or ignored for PH regulation activation. This depends on KLV_HED_DIS NVM bit programming.

In case one of these thresholds is not crossed by PH signal and B+ > set point (VBSPLINRG/VBSPDEF), Phase regulation function is activated.

While phase regulation is active:

- If B+ voltage is greater than set point voltage, EXC DC start from 25 % and increase by steps of 0.78 % every regulation period. This raising transient continues up to a maximum value of 50 %.
- If B+ voltage is smaller than set point voltage, EXC DC is determined by the regulation loop.

While Phase regulation is active, EXC signal behavior when B+ > V_{B+_LIM} depends on OV_LIM_EN NVM bit. When this is set to 0 and B+ > V_{B+_LIM}, EXC DC is set to PWM_NRMAX (NVM bits).

When OV_LIM_EN is set to 1 and B+ > V_{B+_LIM}, EXC DC is set to 0.

Phase regulation behavior respect to overvoltage function limit (U_FELD_AUS) can be selected through LD_NR_DIS NVM bit.

While PH regulation function is active, LIN feedback on EXC DC can be chosen by DC_PHREG NVM bits.

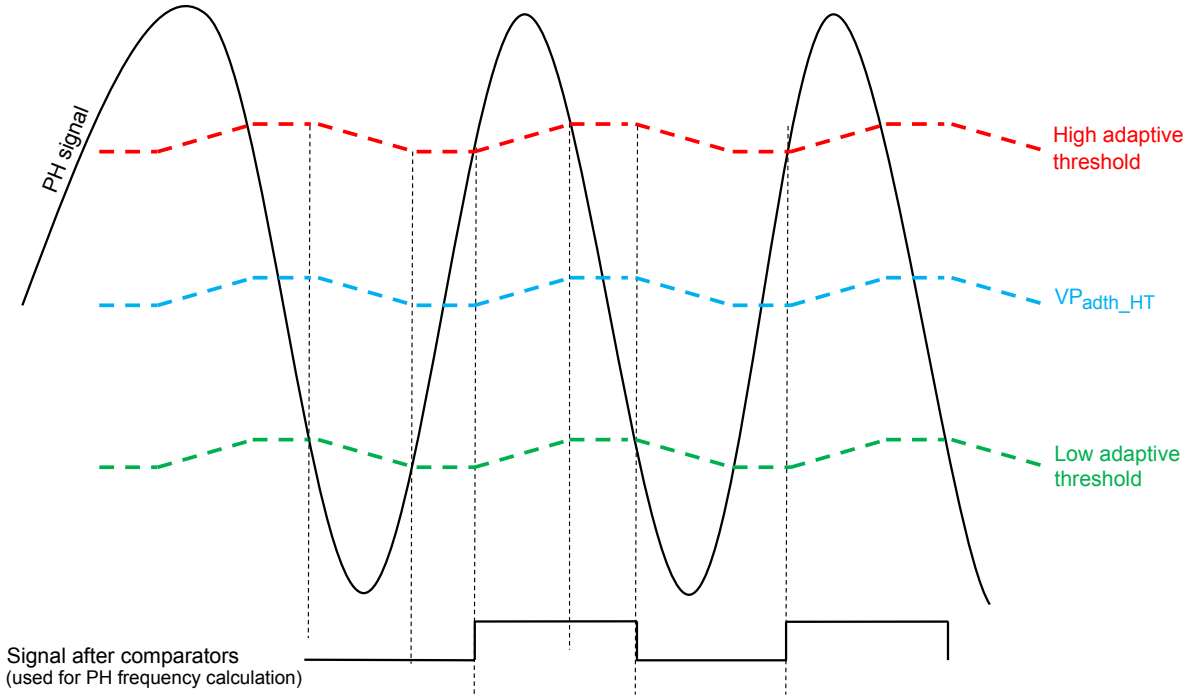
3.2.3 Adaptive PH threshold calculation

L9918 is featured with an adaptive calculation system of PH signal threshold.

The aim of this system is to properly measure PH period and PH amplitude whatever the PH signal average value is.

Picture below shows PH frequency calculation strategy using the adaptive PH thresholds.

Figure 10. **PH frequency calculation using adaptive PH thresholds calculation**



NVM parameters for Adaptive PH thresholds control are: ACADAPMIN_MODE, KLV_AC_ADAP_MAX, KLV_AC_ADAP_MIN and AC_ADAP_M_BAND. Parameters descriptions are reported into Section A.1 NVM parameters table

A further usage of the adaptive PH threshold calculation regards the hot start function activation: one of hot start activation conditions requires Adaptive PH mean value to be greater than VPadth _HT.

A more detailed description of the hot start function can be found into Section 3.2.4 Hot start.

3.2.4 Hot start

Hot start is a particular function which leads device into Regulation default state from Wake up state.

Hot start is activated when the all the three following conditions are verified:

- Phase signal is present on PH pin within 53ms after a wakeup event (Section 1.5.1 Standby).
- Engine rotation is N > N_{start}.
- Adaptive PH threshold mean is greater than $VP_{adth\ \_HT}$ or PH signal crosses phase regulation thresholds ($VP_{HThREG,x}$ threshold and eventually VP_{LTh} if KLV_HED_DIS = 0).

Please note that in case all conditions for Hot Start are met, L9918 however needs a latency time before starting the regulation. This is the time needed to properly evaluate phase signal frequency and it can be programmed by PRG_EVENTFILT_5_3 NVM register.

4 High side driver output - EXC pin

Unless otherwise specified, all the electrical characteristics provided in this chapter refers to T_j between -40 °C and 150 °C.

4.1 EXC electrical characteristic

Table 9. EXC electrical characteristics

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit
Ron	Ron excitation driver	T_j = 150 °C; I_{sunk} = 5 A			0.1	Ω
$VF_{circuit}$	Freewheeling circuit	$I_{sourced}$ = 5 A	-1.5		-0.1	V
IF_{leak}	EXC leakage current	VB+ = 50 V; VF = 0 V	-15		0	µA
IFELD_MAXB1	Excitation driver default current limitation thresholds (IFELD_MAXB NVM bits)	Tj = 25 °C		13		A
IFELD_MAXB2		Tj = 25 °C		I_max value (NVM)		A
IFELD_MAXB3		Tj = 25 °C		11		A
IFELD_MAXB4		Tj = 25 °C		12		A
$IF_{meas\_acc,1}$	Excitation driver current sense and current limitation accuracy	0 < IEXC < 4 A	-0.2		+0.2	A
$IF_{meas\_acc,2}$		4 < IEXC < 11 A	-5		5	%
$IF_{meas\_acc,3}$		11 < IEXC < 13 A	-8		8	%
$IF_{LIM\_LDslope}$	Current limitation threshold slope when device passes from LIN to default regulation		0.337	0.375	0.413	A/s
IF_{OCP}	Excitation driver overcurrent protection value	Tj = 25 °C	13	15	17	A
TF_{OC_filter}	Over-current filter time		6	7	8	µs
VF_{ONdet}	Voltage threshold ON-state detection		0.9	1.1	1.3	V
VF_{ONdet_hyst}	Hysteresis on voltage threshold ON-state detection		0.6	0.65	0.7	V
$fF_{SW,1}$	EXC switching frequency(PWM_FREQ)		190	200	210	Hz
$fF_{SW,2}$			228	240	252	Hz
$fF_{SW,3}$			285	300	315	Hz
$fF_{SW,4}$			380	400	420	Hz
$fF_{SWpreexc}$	EXC switching frequency in pre-excitation		23.75	25	26.25	Hz
SRfall	Falling voltage slew rate for excitation driver	VB = 14 V, R = 270 Ω (Measurement, performed between 80 % and 20 % of the slope with NVM bits any SR_EXC)	0.8	1.9	3	V/µs

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit
SRrise	Rising voltage slew rate for excitation driver	VB = 14 V, R = 270 Ω (Measurement is performed between 20 % and 80 % of the slope with NVM bits any SR_EXC)	0.8	1.9	3	V/µs
$TF_{LRCUP,1}$	Load Response Control Time: rise time (from 0 % to 100 % DC) in default mode (LRD_DEF NVM bits)		0.9	1	1.1	s
$TF_{LRCUP,2}$			1.8	2	2.2	s
$TF_{LRCUP,3}$			2.7	3	3.3	s
$TF_{LRCUP,4}$			3.6	4	4.4	s
$TF_{LRCUP,5}$			4.5	5	5.5	s
$TF_{LRCUP,6}$			5.4	6	6.6	s
$TF_{LRCUP,7}$			6.3	7	7.7	s
$TF_{LRCUP,8}$			7.2	8	8.8	s
$TF_{LRCDW,1}$	Load Response Control Time: return value (from 100 % to 0 % DC) in default mode (LR_TV_INTEGTIME NVM bits)			0.4		s
$TF_{LRCDW,2}$				0.8		s
$TF_{LRCDW,3}$				1.2		s
$TF_{LRCDW,4}$				1.6		s
$TF_{LRCDW,5}$				2.0		s
$TF_{LRCDW,6}$				2.5		s
$TF_{LRCDW,7}$				3.0		s
$TF_{LRCDW,8}$				3.2		s
$DF_{LRCBZ,1}$	Blind Zone in default mode selectable by NVM bits (TV_SPRUNG)			0		%
$DF_{LRCBZ,2}$				0.8		%
$DF_{LRCBZ,3}$				1.6		%
$DF_{LRCBZ,4}$				2.4		%
$DF_{LRCBZ,5}$				3.2		%
$DF_{LRCBZ,6}$				4		%
$DF_{LRCBZ,7}$				4.8		%
$DF_{LRCBZ,8}$				5.6		%
$DF_{LRCBZ,9}$				6.4		%
$DF_{LRCBZ,10}$				7.2		%
$DF_{LRCBZ,11}$				8		%
$DF_{LRCBZ,12}$				8.8		%
$DF_{LRCBZ,13}$				9.6		%
$DF_{LRCBZ,14}$				10.4		%
$DF_{LRCBZ,15}$				11.2		%
$DF_{LRCBZ,16}$				12		%
$DF_{LRCBZ,17}$				12.8		%
$DF_{LRCBZ,18}$				13.6		%

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit
$DF_{LRCBZ,19}$	Blind Zone in default mode selectable by NVM bits (TV_SPRUNG)			14.4		%
$DF_{LRCBZ,20}$				15.2		%
$DF_{LRCBZ,21}$				16		%
$DF_{LRCBZ,22}$				16.8		%
$DF_{LRCBZ,23}$				17.6		%
$DF_{LRCBZ,24}$				18.4		%
$DF_{LRCBZ,25}$				19.2		%
$DF_{LRCBZ,26}$				20		%
$DF_{LRCBZ,27}$				20.8		%
$DF_{LRCBZ,28}$				21.6		%
$DF_{LRCBZ,29}$				22.4		%
$DF_{LRCBZ,30}$				23.2		%
$DF_{LRCBZ,31}$				24		%
$DF_{LRCBZ,32}$				24.8		%
$TF_{DC\_min,1}$	Minimum duty cycle (SST_ULIM_TV0_EN)			0		%
$TF_{DC\_min,2}$					8	%
IF_{RO}	Minimum excitation current when EXC duty cycle is > 40 % for rotor open detection			0.5		A
IMAX_VE1	Excitation Current Limitation in pre-excitation state (IMAX_VE)			Imax_ve_val		A
IMAX_VE2				Imax_ve_val -0.2		A
IMAX_VE3				Imax_ve_val +0.2		A
IMAX_VE4				No Lim		A

EXC duty cycle communication

The duty cycle value applied on the power MOS that drivers the excitation coil of the alternator feeds a digital duty cycle filter.

Table 10. EXC duty cycle communication

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit
$DF_{filter,1}$	EXC duty cycle filter (DFM_FILTER_TP)			13		ms
$DF_{filter,2}$				26		
$DF_{filter,3}$				40		
$DF_{filter,4}$				53		
$DF_{filter,5}$				66		
$DF_{filter,6}$				80		
$DF_{filter,7}$				93		
$DF_{filter,8}$				106		

4.2 EXC characteristics

4.2.1 Minimum and maximum excitation duty cycle:

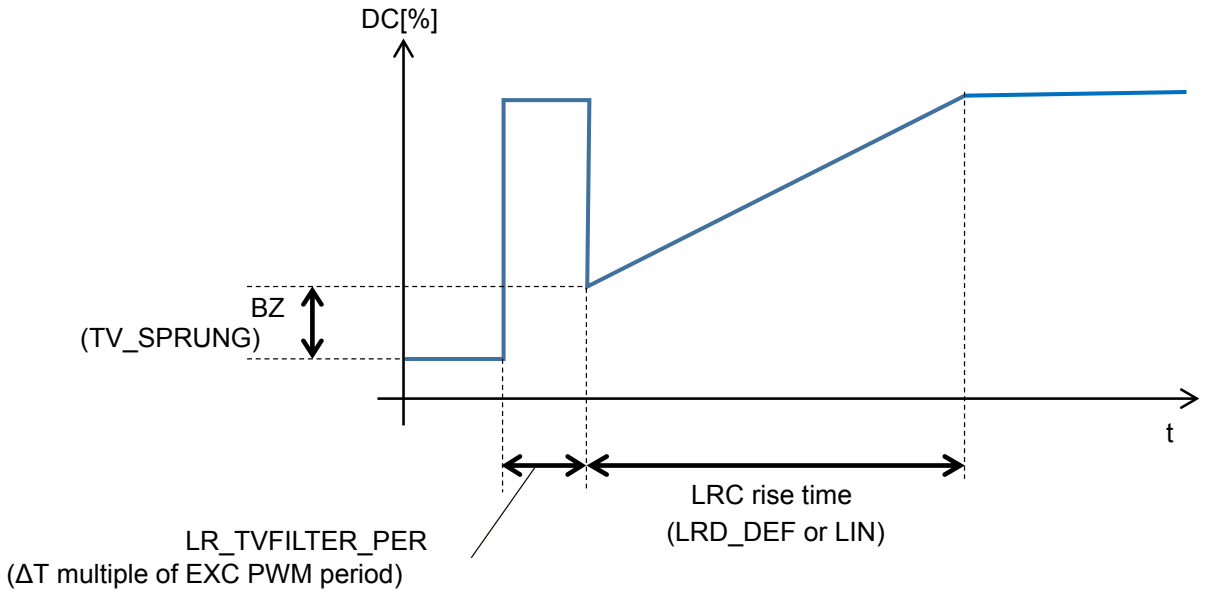
It is possible to set minimum and maximum excitation duty cycle by NVM bits PWM_MINEIN and PWM_MINAUS. Such limits are valid just if the DC calculated by regulation loop is different from 0 % and from 100 %.

4.2.2 Load response control

As previously mentioned, LRC consists in applying a given DC change rate instead of applying the DC calculated by the regulation loop.

Shape of the DC change rate is reported in the picture below:

Figure 11. Load response control



LRC rise time can be set by LIN or by LRD_DEF NVM bits. It is defined as the transient time needed to pass from DC = 0 % condition to DC = 100 % condition.

LRC function is disabled if PH rotation is higher than LRC cut-off threshold. Such threshold can be selected by LIN or by NVM bits LRDN_DEF. Default value selected by NVM programming is ignored in case a valid cut-off frequency is provided through LIN communication.

Other LRC options selectable by NVM bits are: LR_TVFILT_SEL, LR_TVFILTTIME, LR_TVFILTER_PER. Further details on these parameters can be found in table reported into appendix A1.

LRC operation is terminated as soon as DC given by LRC slope becomes higher that the DC calculated by the regulation loop. When this condition occurs, DC calculated by regulation loop is adopted.

Blind Zone control:

Blind Zone control by LIN communication can be enabled by NVM bit TV_SPRUNG_EN. If TV_SPRUNG_EN = 0, device blind zone correspond to the programmed default value DF_{LRCBZ} value.

In case TV_SPRUNG_EN = 1, blind zone can be selected by LIN RX frame. RX frame field available for blind zone control depend on the specific LIN configuration adopted.

4.2.3 Pre-excitation specific mode selection

Short description of NVM settings related to Pre-excitation state has been provided in Section 1.5.3 Pre-excitation.

In this paragraph is reported a more detailed description of the device behavior when Pre-excitation specific mode is selected (SV_FORD_EN = 1). When this setting is adopted, the device has different behaviors depending on set-point voltage sent via LIN communication.

Following lists reports feature and functions active during the pre-excitation in case VBSPLINRG < VB and in case VBSPLINRG > VB respectively.

VBSPLINRG < VB+:

- EXC duty cycle fixed to 25% (except in case current limitation active).
- LRC function disabled.
- Phase regulation disabled.
- Default Excitation current limitation selectable with NVM bit selection (IMAX_VE).
- Safety function enabled.

To be noted that in this case current limitation threshold can't be set by LIN communication. It can just be set by NVM programming.

VBSPLINRG > VB+:

- EXC duty cycle goes to 100% (except in case current limitation active).
- LRC function enabled without LRC return (LRC return value=0s);
- Phase regulation disabled
- Default Excitation current limitation selectable with NVM bit selection (IMAX_VE)
- Excitation current limitation by LIN protocol enabled, so LIN protocol can impose a lower current limitation value.
- Safety function enabled.

Figure 12 and 13 reports two examples of device behavior when SV_FORD_EN = 1.

It can be noticed that while VBSPLINRG < B+, EXC DC remains steady to 25%. While VBSPLINRG > B+, EXC duty cycle is affected by LRC and current limitation function. When these functions are not applied, EXC DC goes to 100%.

Figure 12. Pre-excitation specific mode: example 1

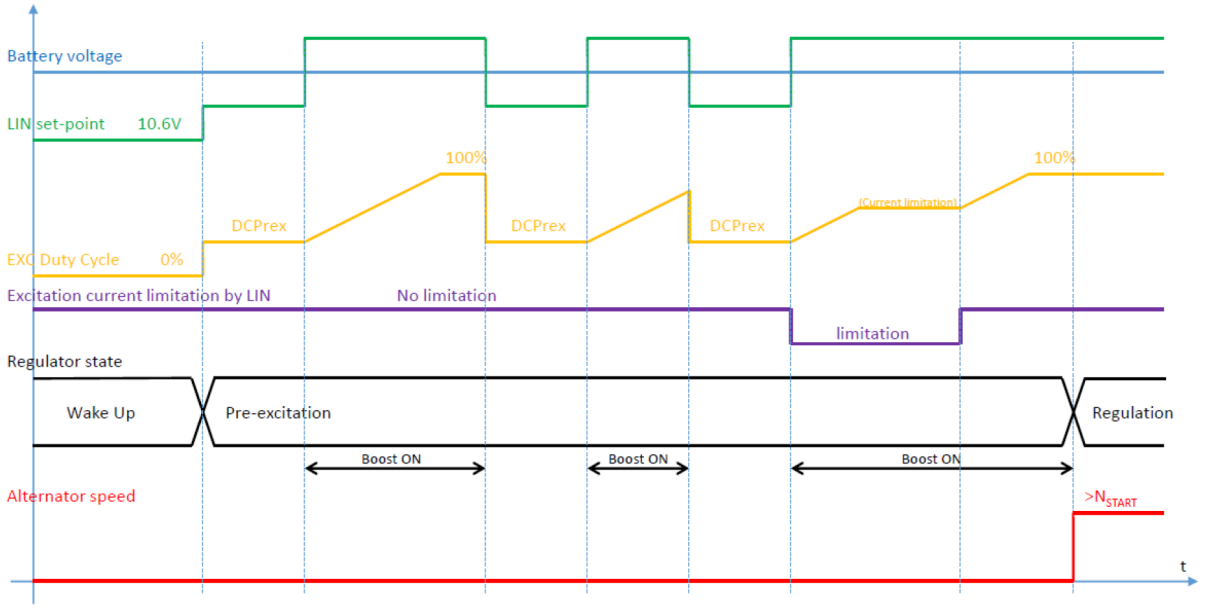
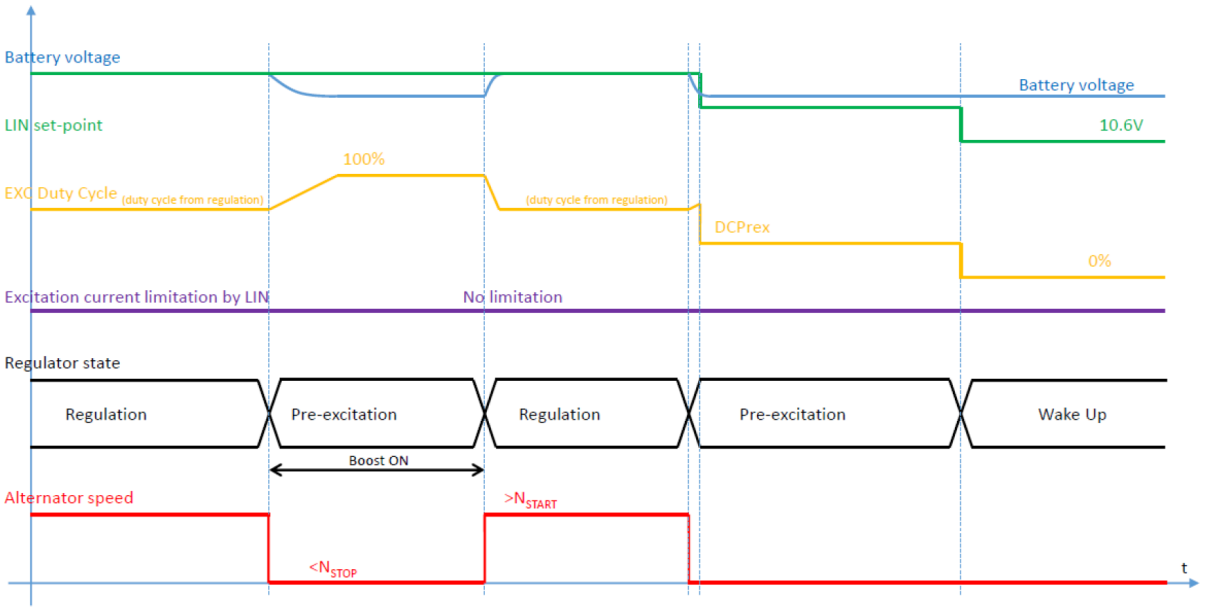


Figure 13. **Pre-excitation specific mode: example 2**



4.2.4 Excitation OFF command

Behaviour of EXC signal in case of VBSPLINRG = 10.6 depends on REG_AUS NVM bits programming into NVM.

Here below a short description of the device behavior for all the possible REG_AUS selection:

- REG_AUS = 0x00: EXC DC is set to 0 % in case N < N_{start} and VBSPLINRG = 10.6. In case N > N_{start} (regulation state) the regulator uses 10.6 as a valid set point and it try to regulate B+ to that target.Once the EXC OFF command is receipt, EXC power stage is kept in OFF until a different VBSPLINRG is received, independently of the PH signal.
- REG_AUS = 0x01: When VBLINSPRG = 10.6, EXC power stage is switched OFF. EXC signal DC remains to 0 % until the OFF command is removed (VBSPLINRG ≠ 10.6).
- REG_AUS = 0x02:EXC DC is set to 0 % in case N < Nstart and VBSPLINRG = 10.6. In case N > N_{start} (regulation state) the regulator uses 10.6 as a valid set point and it try to regulate B+ to that target. Once the EXC OFF command is receipt, EXC power stage is kept in OFF state independently of the PH signal. After 2.5 minutes L9918 restart the regulation if a valid phase signal (N > N_{start}) is detected on PH pin.In any moment the EXC OFF condition can be removed by sending VBSPLINRG ≠ 10.6.
- REG_AUS = 0x03:Same as for REG_AUS = 0x02, the only difference is that the OFF state is 5 minutes long instead of 2.5.

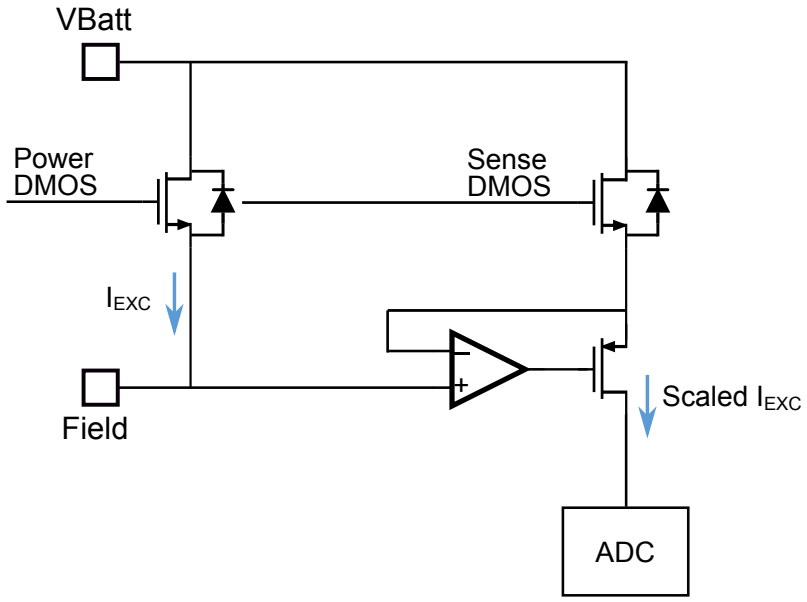
4.2.5 Excitation behavior during phase regulation

The phase regulation function starts if the phase signal has low voltage amplitude. Please refer to Section 3.2.2 Phase regulation for detailed behaviour description.

4.2.6 Excitation current measurement

The excitation current measure is performed sensing the current flowing in the HS power that drives the EXC pin. The working principle is showed in Figure 14.

Figure 14. **Excitation high side power MOS current measurement: working principle**



If the current measured on EXC pin is greater than IF_{OCP} for more than TF_{OC_filter}, overcurrent event is detected and EXC duty cycle is set to 0 %.

Overcurrent flag can be enabled or disabled depending by OVC_FLAG_EN NVM bit programming.

During overcurrent event the device retry EXC power stage activation accordingly to EXC PWM period.

4.2.7 Current limitation

In some cases it is needed to limit the torque required by the alternator to the engine. A direct way to do that is to limit the EXC current flowing into the rotor.

Once a current limitation threshold has been set by LIN or by default (I_MAX, IFELD_MAXB NVM bits), L9918 adjust its output (i.e. its EXC DC) so to do not overcome the limit.

Adopted Current limitation threshold is the lower between default and LIN thresholds.

During its usual functioning, EXC DC is driven by voltage regulation loop control, whose target is to maintain a certain voltage (set point) on car loads. As soon as the EXC current overcome the current limitation threshold, EXC duty cycle is not calculated by voltage regulation loop anymore. Current limitation regulation become dominant and the EXC DC is calculated by current limitation block, whose target is to keep EXC current fixed to the selected threshold.

L9918 can implement current limitation by two different strategies, selectable by ILIM_MODE NVM bit:

- Current limitation regulation loop: is the strategy implemented when ILIM_MODE = 0.

  When this setting is chosen, current regulation is performed by an internal PI loop, whose parameters can be fully programmable by NVM bits (IE_I_ANT, IE_P_ANT and IE_P_ANT_PRE for pre-excitation).
- Fixed DC slope regulation: DC variation is performed applying a fixed slope, selectable by IE_GR_RAMPE NVM bits.

A fixed offset on current limitation threshold can be selected by IFELD_OFFSET NVM bits.

Current limitation is available even into pre-excitation state.

5 Communication terminal - LIN pin

The communication interface implemented in L9918 LIN regulator is compliant with the data link layer specification 1.3, 2.1, 2.2 and 2.2 A. Data exchange via the serial bidirectional bus uses master-slave principle; engine/energy management unit (ECU) is the master and L9918 is the slave.

Lin Slave implemented in L9918 will be able to communicate with following masters:

- LIN Master 1.3
- LIN Master 2.1
- LIN Master 2.2
- LIN Master 2.2 A

The regulator is certified to be compliant to:

- Physical layer compliance with LIN specification 2.2 A. This ensures the possibility for L9918 to communicate with devices compliant with prior LIN Physical Layer specifications.
- Data link layer compliance with LIN specification 1.3, 2.1, 2.2 and 2.2 A.
- Tests defined by LIN Conformance Test Specification Package for LIN 2.2

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Protocol effectively used during the product life is selected by customer by NVM bits (LIN_MODE, LIN_WAKEUP_PATTERN, LIN21_SOFTID_DIS).

LIN communication addresses two different needs for the device: ECU communication during the product life into the brush holder and communication with LIN master for NVM bits programming. In this last case the LIN master is typically represented by a PC and the NVM programming of the device programming registers (listed into Section A.1 NVM parameters table) is typically done at EOL, one time only.

5.1 LIN Physical layer

Physical layer parameters not listed here are implemented according to the LIN2.1 specification

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit
$V_{LINRange}$	Operating voltage range		8		18	V
R_{pu}	Internal pull-up resistor (LIN slave)		20	40	60	kΩ
C_{Slave}	Parasitic LIN capacitance			100	120	pF
I_{LIN_lim}	Current limitation	Dominant state, VB+ = 18 V,Parameter tested while device is transmitting	40		200	mA
$I_{LIN\_PAS\_dom}$	Input leakage current	VLIN = 0 V, VB+ = 12 V,Dominant state, parameter tested while device is not transmitting	-1	-0.3		mA
$I_{LIN\_PAS\_rec}$	Input leakage current	Recessive state,8 V < VLIN < 18 V 8 V < VB+ < 18 V VLIN > VB+	-20		20	µA
$I_{LIN\_NO\_GND}$	Input current if GND is lost	GND disconnected; GND = V_{B+} = 12 V; V_{LIN} = 0 .. 18 V	-1		1	mA
$I_{LIN\_NO\_B+}$	Input current if B+ is lost	B+ disconnected; GND = V_{B+} = 0 V; V_{LIN} = 0 .. 18 V			100	µA
V_{th_dom}	Receiver threshold voltage recessive to dominant state		0.4 * B+	0.45 * B+	0.5 * B+	V

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit
V_{Busdom}	Receiver dominant state				0.4 * B+	V
V_{th_rec}	Receiver threshold voltage dominant to recessive state)		0.5 * B+	0.55 * B+	0.6 * B+	V
V_{Busrec}	Receiver recessive state		0.6 * B+			V
V_{LIN_CNT}	Centering $V_{LIN\_CNT} = (V_{th\_dom} + V_{th\_rec})/2$		0.475 * B +	0.5 * B+	0.525 * B +	V
V_{th_HYS}	Receiver hysteresis $V_{th\_HYS} = V_{th\_rec} - V_{th\_dom}$		0.07 * B+	0.1 * B+	0.175 * B +	V
t_{BFS}	Accuracy of the byte field detection				2/16	Bit time
t_{EBS}	Earliest bit sample time tEBS ≤ tLBS		7/16			Bit time
t_{LBS}	Latest bit sample time tLBS ≥ tEBS				8/16	Bit time
t_{WUDEL}	Time for valid LIN communication after Wake up event		208			µs
V_{THwkup}	Activation threshold for wake-up comparator		1.0	1.5	2	V
$V_{THwkdwn}$	Activation threshold for wake-up comparator		(B+) - 3.5	(B+) - 2.5	(B+) - 1.5	V
t_{LINBUS}	LIN Bus Wake-up Dominant Filter time	Sleep mode; edge: rec-dom		64		µs
t_{dom_LIN}	LIN Bus Wake-up Dominant Filter time	Sleep mode; edge: rec-dom-rec	56			µs
D1	Duty cycle D1 Valid for 20 kBaud	$TH_{REC(max)} = 0.744 * V_{B+}$, $TH_{DOM(max)} = 0.581 * V_{B+}$, V_{B+}=7.0 V to 18 V, t_{BIT} = 50 µs, D1 = $t_{BUS\_rec(min)}$ / (2*tBIT) (1)	0.396			%
D2	Duty cycle D2 Valid for 20 kBaud	$TH_{REC(min)} = 0.422 \times V_{B+}$, $TH_{DOM(min)} = 0.284 \times V_{B+}$, V_{B+} = 7.6 V to 18 V, t_{BIT} = 50 µs, D2 = $t_{BUS\ -\ rec(max)}$ / ($2t_{BIT}$) (1)			0.581	%
D3	Duty cycle D3 Valid for 10.4 kBaud	$TH_{REC(max)} = 0.778 \times V_{B+}$, $TH_{DOM(max)} = 0.616 \times V_{B+}$, V_{B+} = 7.0 V to 18 V, t_{BIT} = 96µs, D3 = $t_{BUS\ -\ rec(min)}$ / ($2t_{BIT}$) (1)	0.417			%
D4	Duty cycle D4 Valid for 10.4 kBaud	$TH_{REC(min)} = 0.389 \times V_{B+}$, $TH_{DOM(min)} = 0.251 \times V_{B+}$, V_{B+} = 7.6 V to 18 V, t_{BIT} = 96µs, D4 = $t_{BUS\ -\ rec(max)}$ / ($2t_{BIT}$) (1)			0.59	%

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit
t_{rx_pd}	Propagation delay of receiver	(T_{RX_PD} = MAX (t_{REC_PDR}, t_{REC_PDF})) (internal timing, from physical layer to data layer logic)			6	µs
t_{rx_sym}	Symmetry of receiver propagation delay rising edge w.r.t. falling edge	(T_{RX_SYM} = t_{REC_PDF} - t_{REC_PDR})	-2		2	µs
$LIN_{autobaud\_range}$	Baud rate selection on transceiver	Automatic selection of one of the baud rate slots	1		20	kHz
t_{LIN_COM}	LIN COM timeout			3		s
$t_{LIN\_to,1}$	Timeout LIN	LIN 1.3		25000		Bit time
$t_{LIN\_to,2}$		LIN 2.x	4	5	10	s

1. *Bus load conditions (CBUS ; RBUS): 1nF; 1kΩ / 6,8nF;660Ω / 10nF;500Ω*

5.2 Message frames

Every data transfer is initiated from the master by sending a “header”. This header contains a synch-break field, a synch byte and a frame identifier byte. The frame identifier byte defines the response, which is sent by the master (RX) or the slave (TX) immediately after the header. The response contains 1 to 8 data bytes and one checksum byte (end of frame). Communication protocol of the regulator implements only 2, 4 and 8 bytes responses.

The producer of any information is called “Publisher” and the consumer of this information is called “Subscriber”.

Except the synch-break field, LIN frames are byte oriented and the LIN specification allows a delay between bytes (inter-byte delay). Every byte consists of a start bit, 8 data bits and one stop bit. Bits are encoded with value 0 (dominant) or 1 (recessive). The LSB is the first bit and the MSB the last bit in a bit stream of a data byte.

5.3 LIN Frames

L9918 addresses many possible frame configurations in order to satisfy requirements coming from many system architectures.

Once a frame configuration is selected, the device is programmed to answer to the correspondent IDs with a specific frame architecture. For example, referring to Table 11, in case LIN1 – Version A is selected, device will answer to the frame IDs reported in the correspondent raw (ID = 29 for RX frame, ID = 11 for TX1 frame etc.). Furthermore the frame architecture (i.e. the reported data, data location into frames etc.) will be compliant with Section 5.3.1.1 Rx Frame version-A description.

LIN frames configuration can be selected by NVM (LIN_CFG) to fit the largest number of applications. Table 11 summarizes the fifteen LIN configurations available. Configuration details are listed in the following tables and their description begins in Section 5.3.1 Message frame for configuration version-A.

Table 11. LIN frame configurations

Version	LIN CFG ID	Frame Type/#Bytes	Identifier Hex
ALL	Accepted only in Wake-UP, Pre-Excitation modes	Rx	3C
		Tx	3D
	Frames Ignored	3E	29
		3F	
Version A	LIN1	Rx_A (4 bytes)	
		Tx_1A (2 bytes)	11
		Tx_2A (2 bytes)	12
		Tx_3A (4 bytes)	15
	LIN2	Rx_A (4 bytes)	2A

Version	LIN CFG ID	Frame Type/#Bytes	Identifier Hex
Version A	LIN2	Tx_1A (2 bytes)	13
		Tx_2A (2 bytes)	14
		Tx_3A (4 bytes)	16
	LIN3	Rx_A (4 bytes)	20
		Tx_1A (2 bytes)	15
		Tx_2A (2 bytes)	21
		Tx_3A (4 bytes)	18
	LIN4	Rx_A (4 bytes)	2A
		Tx_1A (2 bytes)	13
		Tx_2A (2 bytes)	11
		Tx_3A (2 bytes)	16
Version B	LIN1	Rx_B (4 bytes)	29
		Tx_1B (2 bytes)	12
		Tx_2B (4 bytes)	15
	LIN2	Rx_B (4 bytes)	2A
		Tx_1B (2 bytes)	14
		Tx_2B (4 bytes)	16
	LIN3	Rx_B (4 bytes)	20
		Tx_1B (2 bytes)	21
		Tx_2B (4 bytes)	18
	LIN4	Rx_B (4 bytes)	2A
		Tx_1B (2 bytes)	11
		Tx_2B (4 bytes)	16
Version C	LIN	Rx_C (4 bytes)	20
		Tx_1C (4 bytes)	21
		Tx_2C (2 bytes)	18
Version D (with Iexc values)	LIN1	Rx_D (4 bytes)	29
		Tx_1D (2 bytes)	11
		Tx_2D (2 bytes)	12
	LIN2	Rx_D (4 bytes)	2A
		Tx_1D (2 bytes)	13
		Tx_2D (2 bytes)	14
Version D (with Temperature values)	LIN1	Rx_D (4 bytes)	29
		Tx_1D (2 bytes)	11
		Tx_2D (2 bytes)	12
	LIN2	Rx_D (4 bytes)	2A
		Tx_1D (2 bytes)	13
		Tx_2D (2 bytes)	14
Version E	LIN	Rx_E (4 bytes)	29
		Tx_1E (4 bytes)	21
		Tx_2E (2 bytes)	12

Version	LIN CFG ID	Frame Type/#Bytes	Identifier Hex
Version F	LIN	Rx_F (4 bytes)	29
		Tx_1F (2 bytes)	12
		Tx_2F (8 bytes)	15

5.3.1 Message frame for configuration version-A

Next paragraphs provide a description of RX and TX frames available for each selectable LIN configuration.

Indexes reported into the tables are referred to the lists reported into the appendix of this document. These lists provide a full view of all the values which can be sent or received by LIN communication.

For example: suppose in RX frame table the Setpoint (VBSPLINRG) is marked with “A6” signature. This means that the complete list of all the selectable values is reported into “A6” table of the “Set point tables” appendix (see Section A.2).

5.3.1.1 Rx Frame version-A

Table 12. Identifiers: 0x29 (LIN1), 0x2A (LIN2, LIN4), 0x20 (LIN3)

Byte 0								Byte 1								Byte 2								Byte 3							
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
A6						X	X	B1				C1				D5					X	X	X	R			BZ	F			WB

A6: Setpoint (VBSPLINRG), 6 bits

X: Don’t care bits, 2bits

B1: LRC-Rise, 4 bits

C1: LRC-Cut, 4 bits

D5: Excitation Current Limitation, 5 bits

R: Output selection for TxFrame_3/Byte 3, 3 bits

001: VBSPLINRG - Setpoint

010: V_{B+} - Voltage on B+

011: $T_{junction}$ - Junction Temperature

100: Alt. Rotation Speed - Rotation Speed

000/111: RX byte3 invalid

RX: byte3 invalid means BZ, F and BI/BZ bits ignored

BZ: LRC blind zone (feature enabled by TV_SPRUNG_EN NVM register), 1 bit

F: Setpoint limitation threshold for high temperature (delta), 3 bits

WB: Value of this bit changes the proportional constant of the regulation loop (which can be switched between P_ANT and P_ANT2). 1 bit (activity selectable by customer configuration).

5.3.1.2 Tx Frame 1 version-A

Table 13. Identifiers: 0x11 (LIN1), 0x13 (LIN2, LIN4), 0x15 (LIN3)

Byte 0								Byte 1							
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
F_T	F_M	F_E	DCE5					EXC6						F_L1	F_L0

F_T: Diagnosis flag for thermal fault, 1 bit

F_M: Diagnosis flag for mechanical failure, 1 bit

F_E: Diagnosis flag for electrical failure, 1 bit

DCE5: Duty cycle value of the excitation PWM, 5 bits

EXC6: Excitation current measure, 6 bits

L1: Diagnosis flag for LIN error, 1 bit

L0: Diagnosis flag LIN “communication timeout”, 1 bit

5.3.1.3 *Tx Frame 2 version-A*

Table 14. Identifiers: 0x12 (LIN1), 0x14 (LIN2), 0x21 (LIN3), 0x11 (LIN4)

Byte 0								Byte 1							
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
AltS			AltL					DieS			DieL				

AltS: Alternator supplier identification, 3 bits (defined by HER_ID NVM register).

AltL: Alternator identification, 5 bits (defined by GEN_ID NVM register).

DieS: Chip supplier identification, 3 bits (set to 0x3 by EOL programming).

DieL: Chip identification, 5 bits (set to 0x00 by EOL programming).

5.3.1.4 *Tx Frame 3 version-A*

Table 15. Identifiers 0x15 (LIN1), 0x16 (LIN2, LIN4), 0x18 (LIN3)

Byte 0								Byte 1								Byte 2								Byte 3							
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
F_T	F_M	F_E	DCE5					EXC8								RB			F_G	F_H	X	F_L1	F_L0	K							

F_T: Diagnosis flag for thermal fault, 1 bit

F_M: Diagnosis flag for mechanical failure, 1 bit

F_E: Diagnosis flag for electrical failure, 1 bit

DCE5 Duty cycle value of the excitation PWM, 5 bits

EXC8: Measured excitation current, 8 bits

RB: Confirmation of the selected output variable done in RxFrame Byte 3, 3 bits Selected code = Confirmation code

000: RX byte 3 invalid (all bits set as dominant)

001: Vset point feedback (VSPFBK8 table)

010: Vmeas (BV8 table)

011: Tjunction (TJ8 table)

100: Alt. rotation speed (RPM8 table)

101: 00000000

110: reserved

111: RX byte3 invalid

(RX byte3 invalid means BZ, F and BI/BZ bits ignored)

F_G: IEXC flag: current limitation flag, 1 bit (enabled by programming)

F_H: LRC flag: LRC function flag, 1 bit (enabled by programming)

X: Bit answered as “dominant”, 1 bit

F_L1: Diagnosis flag for LIN error, 1 bit

F_L0: Diagnosis flag LIN communication timeout, 1 bit

K: Setpoint/battery voltage/chip temperature/alternator speed, 8 bits, see Section 5.3.1.1

5.3.2 Message frame for configuration version-B

5.3.2.1 Rx Frame version-B

Table 16. Identifiers: 0x29 (LIN1), 0x2A (LIN2, LIN4), 0x20 (LIN3)

Byte 0								Byte 1								Byte 2								Byte 3							
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
A8								B2				C1				X	D7							RB			BZ	F			WB

A8: Setpoint (VBSPLINRG), 8 bits

B2: LRC-Rise, 4 bits

C1: LRC-Cut, 4 bits

X: Don’t care bit, 1 bit

D7: Excitation Current Limitation, 7 bits

RB: Output selection for TxFrame_2/Byte 3 Section 5.3.1.4 , 3 bits

BZ: LRC blind zone (feature enabled by TV_SPRUNG_EN NVM register), 1 bit

F: Setpoint limitation threshold for high temperature (delta), 3 bits

WB: Regulation loop parameters change to optimize the regulation Without Battery 1 bit (activity selectable by customer configuration).

5.3.2.2 Tx Frame 1 version-B

Table 17. Identifiers: 0x12 (LIN1), 0x14 (LIN2), 0x21 (LIN3), 0x11 (LIN4)

Byte 0								Byte 1							
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
AltS			AltL					DieS			DieL				

AltS: Alternator supplier identification, 3 bits (defined by HER_ID NVM register).

AltL: Alternator identification, 5 bits (defined by GEN_ID NVM register).

DieS: Chip supplier identification, 3 bits (set to 0x3 by EOL programming).

DieL: Chip identification, 5 bits (set to 0x00 by EOL programming).

5.3.2.3 *Tx Frame 2 version-B*

Table 18. Identifiers: 0x15 (LIN1), 0x16 (LIN2, LIN4), 0x18 (LIN3)

Byte 0								Byte 1								Byte 2								Byte 3							
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
F_T	F_M	F_E	DCE5					EXC8								RB			F_G	F_H	X	F_L1	F_L0	K							

F_T: Diagnosis flag for thermal fault, 1 bit
F_M: Diagnosis flag for mechanical failure, 1 bit
F_E: Diagnosis flag for electrical failure, 1 bit
DCE5: Duty cycle value of the excitation PWM, 5 bits, see Table 50
EXC8: Measured excitation current, 8 bits, see Table 53
RB: Confirmation of the selected output variable done in Rx frame byte 3, 3 bits
F_G: IEXC flag: current limitation flag, 1 bit (enabled by programming)
F_H: LRC flag: LRC function flag, 1 bit (enabled by programming)
X: Bit answered as “dominant”, 1 bit
F_L1: Diagnosis flag for LIN error, 1 bit
F_L0: Diagnosis flag LIN communication timeout, 1 bit
K: Setpoint/battery voltage/chip temperature/alternator speed, 8 bits

5.3.3 Message frames for configuration version-C

5.3.3.1 *Rx Frame version-C*

Table 19. Identifier: 0x20 (LIN)

Byte 0								Byte 1								Byte 2								Byte 3							
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
BZ2		X						B3				C2				A8								D8							

BZ2: Blind Zone, 2 bits
X: Don’t care bits, 1 bit
B3: LRC-Rise_3, 4 bits
C2: LRC-Cut_2, 4 bits
A8: Setpoint (VBSPLINRG), 8 bits
D8: Excitation current limitation, 8 bits

5.3.3.2 *Tx Frame 1 version-C*

Table 20. Identifier: 0x21 (LIN)

Byte 0								Byte 1								Byte 2								Byte 3							
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7

F_M	F_E	F_L1	F_L0	F_T	X	X	X	BV8	EXC8	DCE8

F_M: Diagnosis flag for mechanical failure, 1 bit
F_E: Diagnosis flag for electrical failure, 1 bit
F_L1: Diagnosis flag for LIN error, 1 bit
F_L0: Diagnosis flag LIN communication timeout, 1 bit
F_T: Diagnosis flag for thermal fault, 1 bit
X: Bits answered as “dominant”, 3 bits
BV8: Voltage measure on B+ pin, 8 bits
EXC8: Excitation current measure, 8 bits
DCE8: Excitation duty cycle measure, 8 bits

5.3.3.3 *Tx Frame 2 version-C*

Table 21. Identifier: 0x18 (LIN)

Byte 0								Byte 1							
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
TJ8								AltS			AltI				

TJ8: Junction temperature measure, 8 bits
AltS: Alternator supplier identification, 3 bits (REF: Table 34)
AltI: Alternator identification, 5 bits (defined by customer)

5.3.4 Message frame for configuration version-D

5.3.4.1 *Rx Frame version-D*

Table 22. Identifiers: 0x29 (LIN1), 0x2A (LIN2)

Byte 0								Byte 1								Byte 2								Byte 3							
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
A6						X	X	B1				C1				D5					X	X	X	X	X	X	X	X	X	X	X

A6: Setpoint (VBSPLINRG), 6 bits
B1: LRC-Rise, 4 bits
C1: LRC-Cut, 4 bits
D5: Excitation Current Limitation, 5 bits
X: Don’t care bits, 11 bits

5.3.4.2 *Tx Frame 1 version-D*

Table 23. Identifiers: 0x11 (LIN1), 0x13 (LIN2)

Byte 0								Byte 1							
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
F_T	F_M	F_E	DCE5					EXC6/TJ6						F_L1	F_L0

F_T Diagnosis flag for thermal fault, 1 bit

F_M Diagnosis flag for mechanical failure, 1 bit

F_E Diagnosis flag for electrical failure, 1 bit

DCE5 Excitation duty cycle measure, 5 bits

EXC6/TJ6 Excitation current/Junction temperature measure (1), 6 bits

F_L1 Diagnosis flag for LIN error, 1 bit

F_L0 Diagnosis flag LIN communication timeout, 1 bit

1. *the two different data correspond to two different LIN versions. Desired answer can be chosen by LIN_CFG programming*

5.3.4.3 *Tx Frame 2 version-D*

Table 24. Identifiers: 0x12 (LIN1), 0x14 (LIN2)

Byte 0								Byte 1							
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
AltS			AltI					F_LB	F_LP	F_LC	F_LE	X	X	X	X

AltS: Alternator supplier identification, 3 bits

AltI: Alternator identification, 5 bits (defined by customer)

F_LB: LIN Break short fault, 1 bit

F_LP: LIN ID parity fault, 1 bit

F_LC: LIN Checksum fault, 1 bit

F_LE: LIN Bit error, 1 bit

X: Bits answered as “dominant”, 4 bits

5.3.5 Message frame for configuration version-E

5.3.5.1 *Rx Frame version-E*

Byte 0								Byte 1								Byte 2								Byte 3							
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
A6						X	X	B4				C2				D8								X	X	X	BZ	X	X	X	X

A6: Setpoint (VBSPLINRG), 6 bits
X: Don't care bits, 2 bits
B4: LRC-Rise, 4 bits
C2: LRC-Cut, 4 bits
D8: Excitation current limitation, 8 bits
X: Don't care bits, 3 bits
BZ: LRC blind zone (feature enabled by TV_SPRUNG_EN NVM register), 1 bit
X: Don't care bits, 4 bits

5.3.5.2 *Tx Frame 1 version-E*

Table 25. Identifier: 0x21 (LIN1)

Byte 0								Byte 1								Byte 2								Byte 3							
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
F_T	F_M	F_E	DCE5					EXC8								X	X	X	X	X	X	F_L1	F_L0	TJ8							

F_T: Diagnosis flag for thermal fault, 1 bit
F_M: Diagnosis flag for mechanical failure, 1 bit
F_E: Diagnosis flag for electrical failure, 1 bit
DCE5: Duty cycle value of the excitation PWM, 5 bits
EXC8: Measured excitation current, 8 bits Table 53
X: Bit answered as "dominant", 6 bits
F_L1: Diagnosis flag for LIN error, 1 bit
F_L0: Diagnosis flag LIN communication timeout, 1 bit
TJ8: Junction temperature measure, 8 bits

5.3.5.3 *Tx Frame 2 version-E*

Table 26. Identifier: 0x12 (LIN1)

Byte 0								Byte 1							
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
AltS			AltL					DieS			DieL				

AltS: Alternator supplier identification, 3 bits (defined by HER_ID NVM register).
AltL: Alternator identification, 5 bits (defined by GEN_ID NVM register).
DieS: Chip supplier identification, 3 bits (set to 0x3 by EOL programming).
DieL: Chip identification, 5 bits (set to 0x00 by EOL programming).

5.3.6 Message frame for configuration version-F

5.3.6.1 *Rx Frame version-F*

Table 27. Identifiers: 0x29

Byte 0								Byte 1								Byte 2								Byte 3							
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
A8								B2				C1				X	D7							R			BZ	F			WB

A8: Setpoint (VBSPLINRG), 8 bits

B2: LRC-Rise, 4 bits

C1: LRC-Cut, 4 bits

X: Don't care bit, 1 bit

D7: Excitation Current Limitation, 7 bits

R: 000/111 disable RX frame byte 3. Other values are "don't care", 3 bits

BZ: LRC blind zone (feature enabled by TV_SPRUNG_EN NVM register), 1 bit

F: Set point limitation threshold for high temperature (delta), 3 bits

WB: Regulation loop parameters change to optimize the regulation Without Battery 1 bit (activity selectable by customer configuration).

5.3.6.2 *Tx Frame 1 version-F*

Table 28. Identifiers: 0x12

Byte 0								Byte 1							
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
AltS			AltI					DieS			DieI				

AltS: Alternator supplier identification, 3 bits

AltI: Alternator identification, 5 bits (defined by customer)

DieS: Chip supplier identification, 3 bits (defined by STM)

DieI: Chip identification, 5 bits (defined by STM)

5.3.6.3 *Tx Frame 2 version-F*

Table 29. Identifiers 0x15

Byte 0								Byte 1								Byte 2								Byte 3							
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
F_T	F_M	F_E	DCE5					EXC8								X			F_G	F_H	X	F_L1	F_L0	A8							

Byte 4								Byte 5								Byte 6							
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7

BV8	RPM8	TJ8	

F_T: Diagnosis flag for thermal fault, 1 bit

F_M: Diagnosis flag for mechanical failure, 1 bit

F_E: Diagnosis flag for electrical failure, 1 bit

DCE5: Duty cycle value of the excitation PWM, 5 bits Table 50

EXC8: Measured excitation current, 8 bits Table 53

F_G: IEXC flag: current limitation flag, 1 bit (enabled by programming)

F_H: LRC flag: LRC function flag, 1 bit (enabled by programming)

X: Bit answered as “dominant”, 1 bit

F_L1: Diagnosis flag for LIN error, 1 bit

F_L0: Diagnosis flag LIN communication timeout, 1 bit

A8: Adopted set point, 8bits

BV8: Battery voltage measure, 8bits

RPM8: Alternator rotation frequency measure, 8 bits

TJ8: Junction temperature measure, 8 bits

5.3.7 Measurements filter

5.3.7.1 Excitation duty cycle

Dc on excitation measure available by LIN Tx frames is optionally filtered with respect to actual Dc on excitation value. Filter parameters are configurable by NVM bit (DFM_FILTER_TP).

5.3.7.2 Iexc measurement filter

Iexc measure available by LIN Tx frames is optionally filtered with respect to actual Iexc value. Filter parameters are configurable by NVM bits (IFELD_FILTER).

5.3.7.3 B+ measurement filter

B+ voltage measure available by LIN Tx frames is optionally filtered with respect to actual B+ voltage value. Filter parameters are configurable by NVM bits (BF_FILT/BF_FILT2).

5.3.7.4 Regulation loop parameters

L9918 regulation loop is conceived to be configured to meet the largest application requirements. Active parameter value (eg. LRC-rise, LRC-cut speed) is selected within pre-fixed set of values. Parameters Sets are typically stored in NVM.

Default configuration (static configuration) provides a full set of regulation parameters.

LIN Rx frame (dynamic configuration) can modify available set/value only for some of regulation parameters.

5.4 LIN Diagnostic frames

Other than LIN frames listed in the previous paragraphs, L9918 supports further specific frames, implemented for diagnostic purposes.

Diagnostic frames IDs are defined as listed below:

- Master diagnostic frames: ID = 0x3C. These frames are sent by LIN master and they does not require answer from communication slave.
- Slave response diagnostic frames: ID = 0x3D. These frame are structured similarly to LIN TX frames: LIN master sends the frame header and the slave is required to answer with data bytes.

Diagnostic frames featured into L9918 are described in the following paragraphs.

5.4.1 Sleep frame

LIN Sleep Frame is a Master diagnostic frame carrying the following data bytes.

Table 30. LIN sleep frame

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
0x00	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF

Sleep frame is valid in all the supported DLL versions.

Once this frame has been received, sleep command is effectively applied within 106 ms. This is the latency time needed by the device for decoding the frame and applying the sleep command.

5.4.2 Read by identifier

Read by Identifier is performed sending two consecutive frames.

The first one is a master diagnostic frame (ID = 0x3C) which identify the slave from which the answer is expected:

Table 31. Master diagnostic frame

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
NAD (1)	0x06	0XB2	0x00	Supplier ID LSB (2)	Supplier ID MSB (2)	Function ID LSB (2)	Function ID MSB (2)

1. *NAD is defined into LIN_NAD NVM bits.*
2. *Supplier ID and Function ID are programmed by STM at EOL. They are set to 0x0040 and to 0x0000 respectively.*

The second frame is a Slave response diagnostic (ID = 0x3D) to which the slave answers with the expected information. Frame contents can be “positive” or “negative” whether the devices recognizes or not the NAD carried by the 0x3C master frame.

Table 32. Negative slave answer

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
NAD	0x03	0X7F	0xB2	0x12	0xFF	0xFF	0xFF

Table 33. Positive slave answer

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
NAD	0x06	0XF2	Supplier ID LSB	Supplier ID MSB	Function ID LSB	Function ID MSB	Variant (1)

1. *Variant is defined into LIN_VAR_ID NVM bits.*

Read by Identifier feature is available for LIN2.x versions only.

5.4.3 Assign frame ID

Assign frame ID range is used to set or disable PIDs (IDs with calculated parity) up to four frames. The request shall be structured as shown in below, ID = 0x3C:

Table 34. Assigne frame

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
NAD	0x06	0xB7	0x00	RX new PID	TX1 new PID	TX2 new PID	TX3 new PID

Please note that the provided new PIDs shall be compliant with parity calculation rule stated by LIN DLL standards.

A response shall only be sent if the NAD matches. If successful, L9918 sends below Slave response frame (ID = 0x3D):

Table 35. Response frame

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
NAD	0x01	0xF7	0xFF	0xFF	0xFF	0xFF	0xFF

Notes:

- The assign frame ID range service is only supported in LIN DLL versions newer than 2.1. Users should configure the Assign Frame ID feature with LIN21_SOFTID_DIS.
- New PIDs assigned can't be stored into NVM. They will be lost after POR (i.e. new wakeup) event.

5.5 LIN Fault detection

5.5.1 Mechanical fault (F_M)

When regulator is in pre-excitation mode F_M flag is set to '1'. F_M fault is configured by MECH_ESAUS_DIS and MASK_FMECH NVM bits.

Table 36. F_M configuration

MECH_ESAUS_DIS	MASK_FMECH	Mechanical fault behavior
0	0	F_M = 1
0	1	F_M is set to 1 just in case VBSPLINRG > VB+ and VBSPLINRG ≠10.6 V
1	0	F_M is set to 1 just in case VBSPLINRG ≠ 10.6 V
1	1	F_M is set to 1 just in case VBSPLINRG>VB+ and VBSPLINRG ≠10.6 V

5.5.2 Electrical fault (F_E)

F_E fault signal passes through a digital filter TflagOn. This deglitch time can be selected by LAMP_FILT NVM bits. It has been introduced in order to avoid false indication problems.

Table below lists the possible cases leading to a F_E flag and the correspondent NVM programming.

Table 37. Electrical fault cases

Case	Required NVM programming	Notes
Duty commanded to 0% and VEXC>Vfondet	-	Short-to-battery
PH voltage below KLV_USSW/KLV_NRSW EXC DC = 100%	ANZ_U_LOW1	
PH voltage below KLV_USSW/KLV_NRSW N < Nstart	ANZ_U_LOW2	
EXC current below 500 mA - EXC_DC > 40%	ANZ_FES	Open load
B+ above V_{B+_LIM}	ANZ_OV_LIM	Overvoltage
B+ above U_FELD_AUS	ANZ_OV_EN	Overvoltage
B+ below 11.3 V N > LRC-cut speed	ANZ_GMUS_EN	

Case	Required NVM programming	Notes
Battery under voltage (U_FELD_EIN threshold)	ANZ_LV_EN	Undervoltage
Overcurrent detected (EXC current > IFOCP)	OVC_FLAG_EN	Short-to-GND

5.5.3 Thermal fault (F_T)

A thermal fault is flagged when thermal compensation starts to operate (see Section 2.2.3).

5.5.4 LIN Timeout flag (F_L0)

Time between two consecutive valid messages must be faster than t_{LIN_COM}. If this time is elapsed, the TO flag is raised.

5.5.5 LIN Communication fault flags (F_L1, F_LB, F_LP, F_LC, F_LE)

Some LIN configurations provide error flags by which the LIN communication integrity can be checked. In some configuration all LIN error flags are aggregated into one flag only (F_L1) while in other configurations it is possible to check separately various requirements of the LIN communication (F_LB, F_LP, F_LC, F_LE).

LIN communication error flag

- F_LC: Checksum error detected: A checksum error is detected
- F_LP: ID parity error detected: The parity field (P0 and P1) of a known identifier is wrong
- F_LB: Inconsistent Break Field Error: Edges of the BREAK (or SYNCH-BREAK) field are detected outside the given tolerances
- Stop bit detected: LIN bus line is dominant while stop bit
- “Bit error” detected: The received bit is different from the bit sent

All these faults are aggregated into F_L1 flag. F_L1 flag rises at the occurrence of any of the listed cases.

5.5.6 LRC flag (F_H)

The LRC flag is set to 1 when LRC is active. This feature is enabled by programming LRC_IEXC_FLAG_EN NVM bit.

5.5.7 Excitation current limitation flag (F_G)

Excitation current limitation flag is flagged as soon as the current limitation is activated.

Excitation current limitation flag is set to ‘1’ even if a “No limitation command is sent by LIN”

This flag has to be enabled by NVM bit LRC_IEXC_FLAG_EN.

Please note that Excitation current limitation flag is exclusively related to current limitation threshold commanded by LIN. It is not applied to the default threshold programmed into the NVM.

In other words, in case EXC current is limited to the threshold provided by LIN communication, the flag is set high. In case EXC current is limited to the default value given by IFELD_MAXB and I_MAX NVM registers, I_EXC flag remains low.

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 PENTAWATT In Line package information

Figure 15. **PENTAWATT In Line package outline**

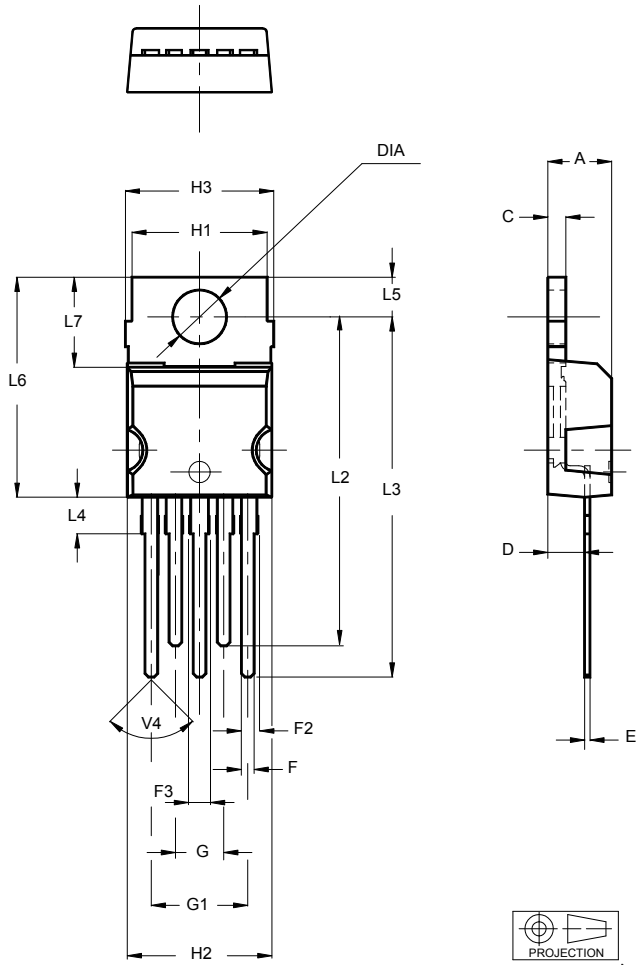

Table 38. **PENTAWATT In-Line package mechanical data**

Symbol	Dimensions mm		
	Min.	Typ.	Max.
A	4.30		4.80
C	1.17		1.37
D	2.40		2.80
E	0.35		0.55
F	0.80		1.05

Symbol	Dimensions mm		
	Min.	Typ.	Max.
F	0.80		0.96
F2	1.10		1.40
F3	1.25		1.55
G	3.20		3.60
G1	6.60		7.0
H1	9.30		9.70
H2			10.40
H3	10.05		10.40
L2	23.05		23.80
L3	25.30		26.10
L4	0.90		2.90
L5	2.60		3.0
L6	15.10		15.80
L7	6.0		6.60
V4		90°	
Dia	3.65		3.85

6.2 Bare die

Die dimension, pads dimension and position will be provided on demand

Appendix A

A.1 NVM parameters table

Table 39. Default mode configuration table

Default values are reported in **bold**.

NVM register name	Definition		Notes	Description
	#Bits	Code		
HER_ID	3	**0x0**	**Bosch**	alternator supplier ID (“AltS” into LIN frames tables)
		0x1	Valeo	
		0x2	Delphi	
		0x3	Hitachi	
		0x4	Denso	
		0x5	Melco	
		0x6	Visteon	
		0x7	Others (JHEECO)	
GEN_ID	5			alternator ID (“AltL” into LIN frames tables)
LIN_MODE	1	**0x0**	**LIN1.3**	LIN protocol variant (2.x means 2.1, 2.2 and 2.2 A protocol versions)
		0x1	LIN2.x	
LIN_WAKEUP_PATTERN	1	0x0	LIN2.2A	LIN wake up event selection
		0x1	Others LIN protocol versions	
LIN21_SOFTID_DIS	1	0x0	enabled	Frame ID service enabled for versions newer than 1.3
		0x1	**disabled**	
LIN_NAD	8			LIN NAD
LIN_CFG	4	**0x0**	**A, LIN1**	LIN frame configuration
		0x1	A, LIN2	
		0x2	A, LIN3	
		0x3	A, LIN4	
		0x4	B, LIN1	
		0x5	B, LIN2	
		0x6	B, LIN3	
		0x7	B, LIN4	
		0x8	C, LIN1	
		0x9	D, LIN1 (with Iexc)	
		0xA	D, LIN2 (with Iexc)	
		0xB	D, LIN1 (with T °C)	
		0xC	D, LIN2 (with T °C)	
		0xD	E, LIN1	
		0xE	F, LIN1	
		0xF	reserved	

NVM register name	Definition		Notes	Description
	#Bits	Code		
TXFRAME_EN	3		TXFRAME_EN(0) = 1 → TX1 enable TXFRAME_EN(1) = 1 → TX2 enable TXFRAME_EN(2) = 1 → TX3 enable. **Default value: 0x7**	TX frames enable
REG_AUS	2	**0x0**	**Power stage off when N < Nstart (regulation voltage = 10.6 V when N > Nstart)regulation is resumed just in case regulation off command is removed**	Set the behavior in case of regulation off command (Vset=10.6 V or REG OFF command via LIN current limitation setting)
		0x1	Power stage off regulation is resumed just in case regulation off command is removed	
		0x2	Power stage off when N < Nstart (regulation voltage = 10.6 V when N > Nstart) regulation is resumed after 2.5 min	
		0x3	Power stage off when N < Nstart (regulation voltage = 10.6 V when N > Nstart) regulation is resumed after 5.0 min	
SR_EXC	2	**0x0**	**480 mA/µs**	EXC current slew rate selection
		0x1	240 mA/µs	
		0x2	360 mA/µs	
		0x3	120 mA/µs	
SR_HT_DIS	1	**0x0**	**Enabled**	Disable of current SR control in case internal temperature greater than Temp_SRctrl.
		0x1	Disabled	
UR_DEF_REG	8		0x00 means 10.6 V, delta voltage is 25 mVsetpoint = code * 0.025 V + 10.6 V (e.g. 0x94 * 0.025 V + 10.6 V = 14.3 V). **Default value: 0x94**	Default regulation setpoint when LIN communication is missing
UR_OFFSET	3	**0x0**	**Disabled**	Fixed set point voltage value correction
		0x1	50 mV	
		0x2	100 mV	
		0x3	150 mV	
		0x4	-50 mV	
		0x5	-100 mV	
		0x6	-150 mV	
		0x7	-200 mV	
REG_PARA_EN	1	**0x0**	**disable**	Enable/disable P_ANT parameter switching via LIN (when enabled, P_ANT2 can be selected via LIN)
		0x1	enable	
P_ANT	5	0x00	0.1 V	Proportional constant of voltage regulation loop (voltage step is 0.1 V)

NVM register name	Definition		Notes	Description
	#Bits	Code		
P_ANT	5	0x01	0.2 V	Proportional constant of voltage regulation loop (voltage step is 0.1 V)
		0x02	0.3 V	
		0x03	0.4 V	
		0x04	**0.5 V**	
		0x05	0.6 V	
		0x06	0.7 V	
		0x07	0.8 V	
		0x08	0.9 V	
		0x09	1.0 V	
		0x0A	1.1 V	
		0x0B	1.2 V	
		0x0C	1.3 V	
		0x0D	1.4 V	
		0x0E	1.5 V	
		0x0F	1.6 V	
		0x10	1.7 V	
		0x11	1.8 V	
		0x12	1.9 V	
		0x13	2.0 V	
		0x14	2.1 V	
		0x15	2.2 V	
		0x16	2.3 V	
		0x17	2.4 V	
		0x18	2.5 V	
		0x19	2.6 V	
		0x1A	2.7 V	
		0x1B	2.8 V	
		0x1C	2.9 V	
		0x1D	3.0 V	
		0x1E	3.0 V	
		0x1F	3.0 V	
P_ANT2	5	0x00	0.1 V	Proportional (direct) control of voltage regulation loop (voltage step is 0.1 V) selectable via LIN
		0x01	0.2 V	
		0x02	0.3 V	
		0x03	0.4 V	
		0x04	0.5 V	
		0x05	0.6 V	
		0x06	0.7 V	
		0x07	0.8 V	
		0x08	0.9 V	

NVM register name	Definition		Notes	Description
	#Bits	Code		
P_ANT2	5	0x09	1.0 V	Proportional (direct) control of voltage regulation loop (voltage step is 0.1 V) selectable via LIN
		0x0A	1.1 V	
		0x0B	1.2 V	
		0x0C	1.3 V	
		0x0D	1.4 V	
		0x0E	1.5 V	
		0x0F	1.6 V	
		0x10	**1.7 V**	
		0x11	1.8 V	
		0x12	1.9 V	
		0x13	2.0 V	
		0x14	2.1 V	
		0x15	2.2 V	
		0x16	2.3 V	
		0x17	2.4 V	
		0x18	2.5 V	
		0x19	2.6 V	
		0x1A	2.7 V	
		0x1B	2.8 V	
		0x1C	2.9 V	
		0x1D	3.0 V	
		0x1E	3.0 V	
		0x1F	3.0 V	
I_ANT	3	0x0	0 mV	Feedback (deviation) control of voltage regulation loop (set point dependency over duty cycle)
		0x1	-50 mV	
		0x2	-100 mV	
		0x3	**-150 mV**	
		0x4	-200 mV	
		0x5	-250 mV	
		0x6	-300 mV	
		0x7	dependency off	
THERMAL_TH_SEL	2	**0x0**	**180 °C**	Thermal shutdown value
		0x1	175 °C	
		0x2	185 °C	
		0x3	190 °C	
I_FILT	4	**0x0**	**180 ms**	Filter time constant of I_ANT feedback for the voltage regulation loop
		0x1	200 ms	
		0x2	220 ms	
		0x3	240 ms	
		0x4	260 ms	

NVM register name	Definition		Notes	Description
	#Bits	Code		
I_FILT	4	0x5	280 ms	Filter time constant of I_ANT feedback for the voltage regulation loop
		0x6	300 ms	
		0x7	320 ms	
		0x8	20 ms	
		0x9	40 ms	
		0xA	60 ms	
		0xB	80 ms	
		0xC	100 ms	
		0xD	120 ms	
		0xE	140 ms	
		0xF	160 ms	
HTK_DIS	1	**0x0**	**enable**	Enable/disable voltage adjustment at high temperature
		0x1	disable	
HT_LIN	1	**0x0**	**disable**	HT cut-off threshold shifting via LIN (HT_KN shifting)
		0x1	enable	
HT_KN	4	0x00	120 °C	Default high temperature threshold over which setpoint is reduced for thermal compensation
		0x01	124 °C	
		0x02	**128 °C**	
		0x03	132 °C	
		0x04	136 °C	
		0x05	140 °C	
		0x06	144 °C	
		0x07	148 °C	
		0x08	152 °C	
		0x09	156 °C	
		0x0A	160 °C	
		0x0B	reserved	
		0x0C	reserved	
		0x0D	reserved	
		0x0E	reserved	
		0x0F	reserved	
HTKMAX_EN	1	**0x0**	**disable**	Enable/disable of the setpoint limitation to 10.6 V in case junction temperature is greater than 176 °C
		0x1	enable	
HT_KN_MAX	2	0x0	160 °C	Maximum threshold value for thermal compensation starting. It is adopted in case HT_KN+LIN offset is greater than HT_KN_MAX
		0x1	164 °C	
		0x2	168 °C	
		0x3	**172 °C**	
HTK_SLOPE	4	**0x0**	**slope = -50.0 mV/°C**	Setpoint value ramp down in case of thermal compensation
		0x1	slope = -100.0 mV/°C	
		0x2	slope = -150.0 mV/°C	

NVM register name	Definition		Notes	Description
	#Bits	Code		
HTK_SLOPE	4	0x3	slope = -200.0 mV/°C	Setpoint value ramp down in case of thermal compensation
		0x4	slope = -250.0 mV/°C	
		0x5	slope = -300.0 mV/°C	
		0x6	slope = -350.0 mV/°C	
		0x7	slope = -400.0 mV/°C	
		0x8	slope = -450.0 mV/°C	
		0x9	slope = -500.0 mV/°C	
		0xA	slope = -550.0 mV/°C	
		0xB	slope = -600.0 mV/°C	
		0xC	slope = -650.0 mV/°C	
		0xD	slope = -700.0 mV/°C	
		0xE	reserved	
		0xF	reserved	
G_HT	2	**0x0**	**50 mV/s**	Setpoint transition gradient in case of thermal compensation
		0x1	25 mV/s	
		0x2	12.5 mV/s	
		0x3	6.25 mV/s	
U_FELD_AUS	2	0x0	16.5 V	Overvoltage function threshold
		0x1	17.0 V	
		0x2	**17.5 V**	
		0x3	18.0 V	
U_FELD_AUS_TIME	2	0x0	520 µs	Filter time of overvoltage function threshold
		0x1	**780 µs**	
		0x2	1040 µs	
		0x3	OV detection deactivated	
U_FELD_EIN	3	0x0	8.75 V	Low voltage function threshold
		0x1	9.25 V	
		0x2	9.75 V	
		0x3	**10 V**	
		0x4	10.25 V	
		0x5	10.5 V	
		0x6	11 V	
		0x7	PSA	
U_FELD_EIN_TIME	2	**0x0**	**520 µs**	Filter time of low voltage function threshold
		0x1	780 µs	
		0x2	1040 µs	
		0x3	1200 µs	
PRIORITY_CH_DIS	1	**0x0**	**enable**	Enable/Disable Low voltage function
		0x1	disable	

NVM register name	Definition		Notes	Description
	#Bits	Code		
PRCH_LRC_EN	1	**0x0**	**disable**	Enable a fixed EXC duty cycle increasing slope when B+ voltage returns over the Low Voltage function threshold (VLOW).
		0x1	enable	
PWM_FREQ	2	**0x0**	**400 Hz**	PWM frequency control
		0x1	300 Hz	
		0x2	240 Hz	
		0x3	200 Hz	
SST_ULIM_TV0_EN	1	**0x0**	**disable**	Enable/disable pre-excitation duty cycle switching to 0% instead of 8% @B+>VB+_LIM
		0x1	enable	
SV_FORD_EN	1	**0x0**	**disable**	Enable/disable pre-excitation special mode
		0x1	enable	
PWM_MINEIN	3	0x0	1	Minimum DC of the EXC signal. If 000 → min DC is (1/128)*100 [%]. If 111 → min DC is (8/128)*100 [%]. Not applied when regulation loop set DC = 100% or DC = 0%.
		0x1	2	
		0x2	3	
		0x3	4	
		0x4	5	
		0x5	**6**	
		0x6	7	
		0x7	8	
PWM_MINAUS	3	0x0	126	Maximum DC of the EXC signal. If 000 → max DC is (126/128)*100 [%]. If 111 → max DC is (119/128)*100 [%]. Not applied when regulation loop set DC = 100% or DC = 0%.
		0x1	125	
		0x2	124	
		0x3	**123**	
		0x4	122	
		0x5	121	
		0x6	120	
		0x7	119	
IFELD_MAXB	2	**0x0**	**13 A**	Excitation current limitation (major priority respect to LIN current limitation threshold)
		0x1	I_MAX	
		0x2	11 A	
		0x3	12 A	
I_MAX	3	0x0	6.0 A	Current limitation threshold
		0x1	7.0 A	
		0x2	8.0 A	
		0x3	**10.0 A**	
		0x4	11.0 A	
		0x5	12.0 A	
		0x6	13.0 A	
		0x7	no limit	
IFELD_OFFSET	3	**0x0**	**Disabled**	Current limitation threshold correction offset

NVM register name	Definition		Notes	Description
	#Bits	Code		
IFELD_OFFSET	3	0x1	50 mA	Current limitation threshold correction offset
		0x2	100 mA	
		0x3	150 mA	
		0x4	-50 mA	
		0x5	-100 mA	
		0x6	-150 mA	
		0x7	-200 mA	
ILIM_MODE	1	0x0	enhanced current limitation	Enhanced current limitation mode switching
		0x1	old current limitation	
IE_I_ANT	5	0x00	disabled	Integral part of current limitation regulation control loop
		0x01	tau = 106 ms	
		0x02	tau = 213 ms	
		0x03	**tau = 320 ms**	
		0x04	tau = 426 ms	
		0x05	tau = 533 ms	
		0x06	tau = 640 ms	
		0x07	tau = 746 ms	
		0x08	tau = 853 ms	
		0x09	tau = 960 ms	
		0x0A	tau = 1066 ms	
		0x0B	tau = 1173 ms	
		0x0C	tau = 1280 ms	
		0x0D	tau = 1386 ms	
		0x0E	tau = 1493 ms	
		0x0F	tau = 1600 ms	
		0x10	tau = 1706 ms	
		0x11	tau = 1813 ms	
		0x12	tau = 1920 ms	
		0x13	tau = 2026 ms	
		0x14	tau = 2133 ms	
		0x15	tau = 2240 ms	
		0x16	tau = 2346 ms	
		0x17	tau = 2453 ms	
		0x18	tau = 2560 ms	
		0x19	tau = 2666 ms	
		0x1A	tau = 2773 ms	
		0x1B	tau = 2880 ms	
		0x1C	tau = 2986 ms	
		0x1D	tau = 3093 ms	
		0x1E	tau = 3200 ms	

NVM register name	Definition		Notes	Description
	#Bits	Code		
IE_I_ANT	5	0x1F	tau = 3306 ms	Integral part of current limitation regulation control loop
IE_P_ANT	7	0x00	not available	Proportional part of current limitation regulation control loop. Referred to regulation mode state.
		0x01	3175 mA	
		0x02	**1587 mA**	
		0x03	1058 mA	
		0x04	794 mA	
		0x05	635 mA	
IE_P_ANT (continued)	7	0x06	529 mA	Proportional part of current limitation regulation control loop. Referred to regulation mode state. (continued)
		0x07	454 mA	
		0x08	397 mA	
		0x09	353 mA	
		0x0A	318 mA	
		0x0B	289 mA	
		0x0C	265 mA	
		0x0D	244 mA	
		0x0E	227 mA	
		0x0F	212 mA	
		0x10	198 mA	
		0x11	187 mA	
		0x12	176 mA	
		0x13	167 mA	
		0x14	159 mA	
		0x15	151 mA	
		0x16	144 mA	
		0x17	138 mA	
		0x18	132 mA	
		0x19	127 mA	
		0x1A	122 mA	
		0x1B	118 mA	
		0x1C	113 mA	
		0x1D	109 mA	
		0x1E	106 mA	
		0x1F	102 mA	
		0x20	99 mA	
		0x21	96 mA	
		0x22	93 mA	
		0x23	91 mA	
		0x24	88 mA	
		0x25	86 mA	

NVM register name	Definition		Notes	Description
	#Bits	Code		
IE_P_ANT (continued)	7	0x26	84 mA	Proportional part of current limitation regulation control loop. Referred to regulation mode state. (continued)
		0x27	81 mA	
		0x28	79 mA	
		0x29	77 mA	
		0x2A	76 mA	
		0x2B	74 mA	
		0x2C	72 mA	
IE_P_ANT (continued)	7	0x2D	71 mA	Proportional part of current limitation regulation control loop. Referred to regulation mode state. (continued)
		0x2E	69 mA	
		0x2F	68 mA	
		0x30	66 mA	
		0x31	65 mA	
		0x32	64 mA	
		0x33	62 mA	
		0x34	61 mA	
		0x35	60 mA	
		0x36	59 mA	
		0x37	58 mA	
		0x38	57 mA	
		0x39	56 mA	
		0x3A	55 mA	
		0x3B	54 mA	
		0x3C	53 mA	
		0x3D	52 mA	
		0x3E	51 mA	
		0x3F	50 mA	
		0x40	50 mA	
		0x41	49 mA	
		0x42	48 mA	
		0x43	47 mA	
		0x44	47 mA	
		0x45	46 mA	
		0x46	45 mA	
		0x47	45 mA	
		0x48	44 mA	
		0x49	43 mA	
		0x4A	43 mA	
		0x4B	42 mA	
		0x4C	42 mA	
		0x4D	41 mA	

NVM register name	Definition		Notes	Description
	#Bits	Code		
IE_P_ANT (continued)	7	0x4E	41 mA	Proportional part of current limitation regulation control loop. Referred to regulation mode state. (continued)
		0x4F	40 mA	
		0x50	40 mA	
		0x51	39 mA	
		0x52	39 mA	
		0x53	38 mA	
IE_P_ANT (continued)	7	0x54	38 mA	Proportional part of current limitation regulation control loop. Referred to regulation mode state. (continued)
		0x55	37 mA	
		0x56	37 mA	
		0x57	36 mA	
		0x58	36 mA	
		0x59	36 mA	
		0x5A	35 mA	
		0x5B	35 mA	
		0x5C	35 mA	
		0x5D	34 mA	
		0x5E	34 mA	
		0x5F	33 mA	
		0x60	33 mA	
		0x61	33 mA	
		0x62	32 mA	
		0x63	32 mA	
		0x64	32 mA	
		0x65	31 mA	
		0x66	31 mA	
		0x67	31 mA	
		0x68	31 mA	
		0x69	30 mA	
		0x6A	30 mA	
		0x6B	30 mA	
		0x6C	29 mA	
		0x6D	29 mA	
		0x6E	29 mA	
		0x6F	29 mA	
		0x70	28 mA	
		0x71	28 mA	
		0x72	28 mA	
		0x73	28 mA	
		0x74	27 mA	
		0x75	27 mA	

NVM register name	Definition		Notes	Description
	#Bits	Code		
IE_P_ANT (continued)	7	0x76	27 mA	Proportional part of current limitation regulation control loop. Referred to regulation mode state. (continued)
		0x77	27 mA	
		0x78	26 mA	
		0x79	26 mA	
		0x7A	26 mA	
IE_P_ANT (continued)	7	0x7B	26 mA	Proportional part of current limitation regulation control loop. Referred to regulation mode state. (continued)
		0x7C	26 mA	
		0x7D	25 mA	
		0x7E	25 mA	
		0x7F	25 mA	
IE_GR_RAMPE	1	**0x0**	**1 decrement(1/128) every regulator period**	Duty cycle decrease slope when current limitation mode is activated.Active when ILIM_MODE = 0x1
		0x1	1 decrement(1/128) every 2 regulator periods	
IMAX_VE	2	0x0	IMAX_VE_VAL	Excitation current limitation in pre-excitation
		0x1	IMAX_VE_VAL - 200 mA	
		0x2	IMAX_VE_VAL + 200 mA	
		0x3	**no limit**	
IMAX_VE_VAL	6		0x00 means 0.0 A, delta voltage is 100 mAIMAX_VE_VAL = code * 0.1 A. **Default set to 0x010.**	Excitation current limitation value in pre-excitation (0.0 A-6.3 A, Δ0.1 A, default 1.0 A)
IE_P_ANT_PRE	7	0x00	not available	Proportional part of current limitation regulation control loop in pre-excitation
		0x01	**3175 mA**	
		0x02	1587 mA	
		0x03	1058 mA	
		0x04	794 mA	
		0x05	635 mA	
		0x06	529 mA	
		0x07	454 mA	
		0x08	397 mA	
		0x09	353 mA	
		0x0A	318 mA	
		0x0B	289 mA	
		0x0C	265 mA	
		0x0D	244 mA	
		0x0E	227 mA	
		0x0F	212 mA	
		0x10	198 mA	
		0x11	187 mA	
		0x12	176 mA	

NVM register name	Definition		Notes	Description
	#Bits	Code		
IE_P_ANT_PRE	7	0x13	167 mA	Proportional part of current limitation regulation control loop in pre-excitation
		0x14	159 mA	
		0x15	151 mA	
		0x16	144 mA	
		0x17	138 mA	
		0x18	132 mA	
		0x19	127 mA	
		0x1A	122 mA	
		0x1B	118 mA	
		0x1C	113 mA	
		0x1D	109 mA	
IE_P_ANT_PRE (continued)	7	0x1E	106 mA	Proportional part of current limitation regulation control loop in pre-excitation (continued)
		0x1F	102 mA	
		0x20	99 mA	
		0x21	96 mA	
		0x22	93 mA	
		0x23	91 mA	
		0x24	88 mA	
		0x25	86 mA	
		0x26	84 mA	
		0x27	81 mA	
		0x28	79 mA	
		0x29	77 mA	
		0x2A	76 mA	
		0x2B	74 mA	
		0x2C	72 mA	
		0x2D	71 mA	
		0x2E	69 mA	
		0x2F	68 mA	
		0x30	66 mA	
		0x31	65 mA	
		0x32	64 mA	
		0x33	62 mA	
		0x34	61 mA	
		0x35	60 mA	
		0x36	59 mA	
		0x37	58 mA	
		0x38	57 mA	
		0x39	56 mA	
		0x3A	55 mA	

NVM register name	Definition		Notes	Description
	#Bits	Code		
IE_P_ANT_PRE (continued)	7	0x3B	54 mA	Proportional part of current limitation regulation control loop in pre-excitation (continued)
		0x3C	53 mA	
		0x3D	52 mA	
		0x3E	51 mA	
		0x3F	50 mA	
		0x40	50 mA	
		0x41	49 mA	
		0x42	48 mA	
		0x43	47 mA	
		0x44	47 mA	
IE_P_ANT_PRE (continued)	7	0x45	46 mA	Proportional part of current limitation regulation control loop in pre-excitation (continued)
		0x46	45 mA	
		0x47	45 mA	
		0x48	44 mA	
		0x49	43 mA	
		0x4A	43 mA	
		0x4B	42 mA	
		0x4C	42 mA	
		0x4D	41 mA	
		0x4E	41 mA	
		0x4F	40 mA	
		0x50	40 mA	
		0x51	39 mA	
		0x52	39 mA	
		0x53	38 mA	
		0x54	38 mA	
		0x55	37 mA	
		0x56	37 mA	
		0x57	36 mA	
		0x58	36 mA	
		0x59	36 mA	
		0x5A	35 mA	
		0x5B	35 mA	
		0x5C	35 mA	
		0x5D	34 mA	
		0x5E	34 mA	
		0x5F	33 mA	
		0x60	33 mA	
		0x61	33 mA	
		0x62	32 mA	

NVM register name	Definition		Notes	Description
	#Bits	Code		
IE_P_ANT_PRE (continued)	7	0x63	32 mA	Proportional part of current limitation regulation control loop in pre-excitation (continued)
		0x64	32 mA	
		0x65	31 mA	
		0x66	31 mA	
		0x67	31 mA	
		0x68	31 mA	
		0x69	30 mA	
		0x6A	30 mA	
		0x6B	30 mA	
IE_P_ANT_PRE (continued)	7	0x6C	29 mA	Proportional part of current limitation regulation control loop in pre-excitation (continued)
		0x6D	29 mA	
		0x6E	29 mA	
		0x6F	29 mA	
		0x70	28 mA	
		0x71	28 mA	
		0x72	28 mA	
		0x73	28 mA	
		0x74	27 mA	
		0x75	27 mA	
		0x76	27 mA	
		0x77	27 mA	
		0x78	26 mA	
		0x79	26 mA	
		0x7A	26 mA	
		0x7B	26 mA	
		0x7C	26 mA	
		0x7D	25 mA	
		0x7E	25 mA	
		0x7F	25 mA	
LRD_DEF	3	0x0	1s	Default load response control (LRC) rise time
		0x1	2s	
		0x2	**3s**	
		0x3	4s	
		0x4	5s	
		0x5	6s	
		0x6	7s	
		0x7	8s	
LRDN_DEF	2	**0x0**	**3000 RPM**	Default load response control (LRC) cut-off speed
		0x1	4000 RPM	
		0x2	4800 RPM	

NVM register name	Definition		Notes	Description
	#Bits	Code		
LRDN_DEF	2	0x3	6000 RPM	Default load response control (LRC) cut-off speed
LR_TV_INTEGTIME	3	**0x0**	**0.4s**	negative load response control (LRC) gradient
		0x1	0.8s	
		0x2	1.2s	
		0x3	1.6s	
		0x4	2.0s	
		0x5	2.5s	
		0x6	3.0s	
		0x7	3.2s	
TV_SPRUNG_EN	1	**0x0**	**disable**	Enable/disable blind zone selecting via LIN
		0x1	enable	
TVSTART25_EN	1	**0x0**	**according to blind zone setting**	Constant start duty cycle of 25% in case of LRC activation when device passes from pre-exctitation state to regulation state
		0x1	DC = 25.0%	
TV_SPRUNG	5	0x00	TV = 0.0%	Default load response control (LRC) blind zone
		0x01	TV = 0.8%	
		0x02	TV = 1.6%	
		0x03	TV = 2.4%	
		0x04	TV = 3.2%	
		0x05	TV = 4.0%	
		0x06	TV = 4.8%	
		0x07	TV = 5.6%	
		0x08	TV = 6.4%	
		0x09	TV = 7.2%	
		0x0A	TV = 8.0%	
		0x0B	TV = 8.8%	
		0x0C	TV = 9.6%	
		0x0D	TV = 10.4%	
		0x0E	TV = 11.2%	
		0x0F	TV = 12.0%	
		0x10	**TV = 12.8%**	
		0x11	TV = 13.6%	
		0x12	TV = 14.4%	
		0x13	TV = 15.2%	
		0x14	TV = 16.0%	
		0x15	TV = 16.8%	
		0x16	TV = 17.6%	
		0x17	TV = 18.4%	
		0x18	TV = 19.2%	
		0x19	TV = 20.0%	

NVM register name	Definition		Notes	Description
	#Bits	Code		
TV_SPRUNG	5	0x1A	TV = 20.8%	Default load response control (LRC) blind zone
		0x1B	TV = 21.6%	
		0x1C	TV = 22.4%	
		0x1D	TV = 23.2%	
		0x1E	TV = 24.0%	
		0x1F	TV = 24.8%	
DFM_START_RAMP	1	**0x0**	**Duty cycle calculated by regulation loop**	Output duty cycle value during LRC
		0x1	Duty cycle calculated by LRC function (real DC value on EXC)	
LR_TVFILT_SEL	1	**0x0**	**high sensitivity (after filter)**	Change sensitivity for load response control (LRC) activation (PWM selection before or after filter)
		0x1	low sensitivity (before filter)	
LR_TVFILTTIME	4	**0x0**	**20 ms**	Filter time constant of duty cycle
		0x1	40 ms	
		0x2	60 ms	
		0x3	80 ms	
		0x4	100 ms	
		0x5	120 ms	
		0x6	140 ms	
		0x7	160 ms	
		0x8	180 ms	
		0x9	200 ms	
		0xA	220 ms	
		0xB	240 ms	
		0xC	2.5 ms	
		0xD	5ms	
		0xE	7.5 ms	
		0xF	10 ms	
LR_TVFILTER_PER	2	0x0	0 period	Number of delayed PWM periods before load response control (LRC) start
		0x1	1 period	
		0x2	**2 periods**	
		0x3	3 periods	
POLZ	3	0x0	5	Poles pair number
		0x1	**6**	
		0x2	7	
		0x3	8	
		0x4	9	
		0x5	reserved	
		0x6	reserved	
		0x7	reserved	

NVM register name	Definition		Notes	Description
	#Bits	Code		
N_NOTSTART	1	**0x0**	**N_NOTSTART_VAL**	Self-start rotation speed threshold
		0x1	4000 RPM	
N_NOTSTART_VAL	6		Speed mapping rule: 255-code*4 → Alternator speed measure table (see Section A.13 Alternator speed measure).For example: default code value = 0xC → 255-code*4 = 207 which correspond to 3000RPM into the “Alternator speed measure table”. **Default value: 0x0C.**	Emergency start speed threshold value
DREHFILT_MODE	1	**0x0**	**enable**	Enable/disable PRG_EVENTFILT_2_0 and PRG_EVENTFILT_5_3
		0x1	disable	
PRG_EVENTFILT_2_0	3	0x0	1	Filter number phase periods for detection: LRC and emergency start speed threshold
		0x1	**3**	
		0x2	5	
		0x3	7	
		0x4	9	
		0x5	11	
		0x6	13	
		0x7	15	
N0_FILTERTIME_SET	2	0x0	0 ms	Filter time before start speed event removal (RPM<Nstart)
		0x1	**50 ms**	
		0x2	100 ms	
		0x3	300 ms	
PRG_EVENTFILT_5_3	3	0x0	0	Number of phase periods for detection before hot start speed event generation
		0x1	1	
		0x2	2	
		0x3	**3**	
		0x4	4	
		0x5	5	
		0x6	6	
		0x7	7	
PHASE_FILT_EN	1	**0x0**	**disable**	Enable first order LPF for phase ADC
		0x1	enable	
KLV_HED_DIS	1	**0x0**	**peak to peak AC threshold**	Phase regulation option to set which thresholds are applied on PH signal - KLV_HED_DIS = 0: high and low thresholds are considered - KLV_HED_DIS = 1: high threshold only is considered
		0x1	peak only AC threshold	
ACADAPMIN_MODE	1	**0x0**	**AC_ADAP_M_BAND value when normal start, KLV_AC_ADAP_MIN_NOT value when emergency start**	Adaptive PH threshold lower saturation value for normal/self-start

NVM register name	Definition		Notes	Description
	#Bits	Code		
ACADAPMIN_MODE	1	0x1	KLV_AC_ADAP_MIN_NOT value for both	Adaptive PH threshold lower saturation value for normal/self-start
KLV_AC_ADAP_MAX	3	0x0	2.5 V	Upper saturation value for PH adaptive threshold
		0x1	3.0 V	
		0x2	3.5 V	
		0x3	4.0 V	
		0x4	4.5 V	
		0x5	5.0 V	
		0x6	5.5 V	
		0x7	**6.0 V**	
KLV_AC_ADAP_MIN	3	0x0	0.2 V	Lower saturation value for PH adaptive thresholdUsage of this parameter depends on ACADAPMIN_MODE
		0x1	0.6 V	
		0x2	**1.0 V**	
		0x3	1.4 V	
		0x4	1.8 V	
		0x5	2.2 V	
		0x6	2.6 V	
		0x7	3.0 V	
AC_ADAP_M_BAND	2	**0x0**	**KLV_AC_ADAP_MIN**	Lower saturation value for PH adaptive thresholdUsage of this parameter depends on ACADAPMIN_MODE
		0x1	1.4 V	
		0x2	1.8 V	
		0x3	2.2 V	
KLV_NRSW	4	0x0	4V	High threshold for the phase regulation when device is operating into regulation state
		0x1	5.5 V	
		0x2	7.0 V	
		0x3	7.7 V	
		0x4	9.0 V	
		0x5	9.5 V	
		0x6	**10.2 V**	
		0x7	10.4 V	
		0x8	10.6 V	
		0x9	10.8 V	
		0xA	11.0 V	
		0xB	11.2 V	
		0xC	11.4 V	
		0xD	11.6 V	
		0xE	11.8 V	
		0xF	12.0 V	
KLV_AC_ADAP_MIN_NOT	3	0x0	0.2 V	Lower saturation value for PH adaptive thresholdUsage of this parameter depends on ACADAPMIN_MODE
		0x1	**0.3 V**	

NVM register name	Definition		Notes	Description
	#Bits	Code		
KLV_AC_ADAP_MIN_NOT	3	0x2	0.4 V	Lower saturation value for PH adaptive thresholdUsage of this parameter depends on ACADAPMIN_MODE
		0x3	0.5 V	
		0x4	0.6 V	
		0x5	0.7 V	
		0x6	0.8 V	
		0x7	0.9 V	
KLV_USSW	4	0x0	6.0 V	High threshold for the phase regulation adopted while device is into Wake Up state.
		0x1	6.2 V	
		0x2	6.4 V	
		0x3	6.6 V	
		0x4	6.8 V	
		0x5	**7.0 V**	
		0x6	7.2 V	
		0x7	7.4 V	
		0x8	7.6 V	
		0x9	7.8 V	
		0xA	8.0 V	
		0xB	8.2 V	
		0xC	8.4 V	
		0xD	8.6 V	
		0xE	8.8 V	
		0xF	9.0 V	
KLV_LOWSW	1	**0x0**	**1.8 V**	Low phase regulation threshold
		0x1	2.0 V	
OV_LIM_EN	1	0x0	disable	Enables EXC shut down in case B+> VB+_lim
		0x1	**enable**	
LD_NR_DIS	1	0x0	phase regulation active	Disabling of OV (B+>U_FELD_AUS) function when device is in phase regulation
		0x1	**phase regulation off**	
DC_PHREG	2	**0x0**	**DC calculated by voltage regulation loop**	Setting of the DC value answered by LIN during phase regulation.
		0x1	25% (Pre-exc DC)	
		0x2	0%	
		0x3	Phase regulation DC (real DC on EXC)	
PWM_NRMAX	3	0x0	TV = 5.5%	EXC duty cycle limitation at B+ > B+_lim during phase regulation
		0x1	TV = 12.0%	
		0x2	TV = 18.0%	
		0x3	**TV = 24.0%**	
		0x4	TV = 31.0%	
		0x5	TV = 37.0%	

NVM register name	Definition		Notes	Description
	#Bits	Code		
PWM_NRMAX	3	0x6	TV = 43.0%	EXC duty cycle limitation at B+ > B+_lim during phase regulation
		0x7	TV = 50.0%	
DFM_FILTER_TP	3	0x0	13 ms	Filter time constant of EXC duty cycle monitor
		0x1	26 ms	
		0x2	**40 ms**	
		0x3	53 ms	
		0x4	66 ms	
		0x5	80 ms	
		0x6	93 ms	
		0x7	106 ms	
BF_FILT	3	0x0	filter time constant tau = 0.8 ms	B+ filter constant of the regulation parameter while P_ANT is used
		0x1	**filter time constant tau = 1.7 ms**	
		0x2	filter time constant tau = 2.5 ms	
		0x3	filter time constant tau = 3.3 ms	
		0x4	filter time constant tau = 4.2 ms	
		0x5	filter time constant tau = 5.0 ms	
		0x6	filter time constant tau = 5.8 ms	
		0x7	filter time constant tau = 6.7 ms	
BF_FILT2	3	**0x0**	**filter time constant tau = 0.8 ms**	B+ filter constant of the regulation parameter while P_ANT2 is used
		0x1	filter time constant tau = 1.7 ms	
		0x2	filter time constant tau = 2.5 ms	
		0x3	filter time constant tau = 3.3 ms	
		0x4	filter time constant tau = 4.2 ms	
		0x5	filter time constant tau = 5.0 ms	
		0x6	filter time constant tau = 5.8 ms	
		0x7	filter time constant tau = 6.7 ms	
IFELD_FILTER	3	**0x0**	**IFELD_FILTER_SEL**	Time constant of the EXC current filter measurement
		0x1	filter time constant tau = 160 ms	
		0x2	filter time constant tau = 66 ms	

NVM register name	Definition		Notes	Description
	#Bits	Code		
IFELD_FILTER	3	0x3	filter time constant tau = 33 ms	Time constant of the EXC current filter measurement
		0x4	filter time constant tau = 13 ms	
		0x5	filter time constant tau = 66 ms	
		0x6	filter time constant tau = 66 ms	
		0x7	filter time constant tau = 66 ms	
IFELD_FILTER_SEL	1	0x0	filter time constant tau = 213 ms	Time constant of the field current filter
		0x1	**filter time constant tau = 106 ms**	
MECH_ESAUS_DIS	1	**0x0**	**disable**	F_M configuration bit (details on Table 36)
		0x1	enable	
MASK_FMECH	1	0x0	disable	F_M configuration bit (details on Table 36)
		0x1	**enable**	
ANZ_LV_EN	1	0x0	disable	Low voltage flag enable
		0x1	**enable**	
ANZ_OV_EN	1	**0x0**	**disable**	Overvoltage flag enable
		0x1	enable	
ANZ_OV_LIM	1	0x0	disable	Overvoltage protection flag enable during phase regulation (OV_LIM_EN = 0x1 required)
		0x1	**enable**	
ANZ_U_LOW1	1	0x0	disable	Enable low voltage flag @EXC_DC = 100% and phase voltage below KLV_USSW/KLV_NRSW
		0x1	**enable**	
ANZ_U_LOW2	1	**0x0**	**disable**	Low voltage flag enable at phase frequency < speed detection threshold (N < Nstart) and phase voltage below KLV_USSW/KLV_NRSW
		0x1	enable	
ANZ_FES	1	0x0	disable	Enable low field current flag @EXC_DC > 40% & IFES < 0.5 A
		0x1	**enable**	
ANZ_GMUS_EN	1	**0x0**	**disable**	Enable GM F_E mode: B+ < 11.3 V && RPM<LRC cut off speed)
		0x1	enable	
KLV_ACWANR_DIS	1	**0x0**	**enable**	Enable/disable of PH amplitude check ((max-min)/ 2>3V) to perform hot start
		0x1	disable	
LAMP_FILT	3	0x0	150 ms	F_E flag filter time
		0x1	1/4 s	
		0x2	**2/4 s**	
		0x3	3/4 s	
		0x4	4/4 s	
		0x5	5/4 s	
		0x6	6/4 s	
		0x7	7/4 s	

NVM register name	Definition		Notes	Description
	#Bits	Code		
ANZ_HT_EN	1	**0x0**	**disable**	Enable thermal compensation flag
		0x1	enable	
OVC_FLAG_EN	1	**0x0**	**disable**	Enabling of overcurrent flag.
		0x1	enable	
LRC_IEXC_FLAG_EN	1	**0x0**	**disable**	Enable LIN LRC_flag and IEXC_flag
		0x1	enable	

A.2 SetPoint tables

Table 40. SetPoint table: 6 bit (A6), 8 bit (A8)

SetPoint (V)	Code6 (A,D,E)	Code8 (B,C, F)	SetPoint (V)	Code6 (A,D,E)	Code8 (B,C, F)
10.600	000000 (OFF)	00000000	13.800	100000	10000000
10.625		00000001	13.825		10000001
10.650		00000010	13.850		10000010
10.675		00000011	13.875		10000011
10.700	000001	00000100	13.900	100001	10000100
10.725		00000101	13.925		10000101
10.750		00000110	13.950		10000110
10.775		00000111	13.975		10000111
10.800	000010	00001000	14.000	100010	10001000
10.825		00001001	14.025		10001001
10.850		00001010	14.050		10001010
10.875		00001011	14.075		10001011
10.900	000011	00001100	14.100	100011	10001100
10.925		00001101	14.125		10001101
10.950		00001110	14.150		10001110
10.975		00001111	14.175		10001111
11.000	000100	00010000	14.200	100100	10010000
11.025		00010001	14.225		10010001
11.050		00010010	14.250		10010010
11.075		00010011	14.275		10010011
11.100	000101	00010100	14.300	100101	10010100
11.125		00010101	14.325		10010101
11.150		00010110	14.350		10010110
11.175		00010111	14.375		10010111
11.200	000110	00011000	14.400	100110	10011000
11.225		00011001	14.425		10011001
11.250		00011010	14.450		10011010
11.275		00011011	14.475		10011011
11.300	000111	00011100	14.500	100111	10011100

SetPoint (V)	Code6 (A,D,E)	Code8 (B,C, F)	SetPoint (V)	Code6 (A,D,E)	Code8 (B,C, F)
11.325		00011101	14.525		10011101
11.350		00011110	14.550		10011110
11.375		00011111	14.575		10011111
11.400	001000	00100000	14.600	101000	10100000
11.425		00100001	14.625		10100001
11.450		00100010	14.650		10100010
11.475		00100011	14.675		10100011
11.500	001001	00100100	14.700	101001	10100100
11.525		00100101	14.725		10100101
11.550		00100110	14.750		10100110
11.575		00100111	14.775		10100111
11.600	001010	00101000	14.800	101010	10101000
11.625		00101001	14.825		10101001
11.650		00101010	14.850		10101010
11.675		00101011	14.875		10101011
11.700	001011	00101100	14.900	101011	10101100
11.725		00101101	14.925		10101101
11.750		00101110	14.950		10101110
11.775		00101111	14.975		10101111
11.800	001100	00110000	15.000	101100	10110000
11.825		00110001	15.025		10110001
11.850		00110010	15.050		10110010
11.875		00110011	15.075		10110011
11.900	001101	00110100	15.100	101101	10110100
11.925		00110101	15.125		10110101
11.950		00110110	15.150		10110110
11.975		00110111	15.175		10110111
12.000	001110	00111000	15.200	101110	10111000
12.025		00111001	15.225		10111001
12.050		00111010	15.250		10111010
12.075		00111011	15.275		10111011
12.100	001111	00111100	15.300	101111	10111100
12.125		00111101	15.325		10111101
12.150		00111110	15.350		10111110
12.175		00111111	15.375		10111111
12.200	010000	01000000	15.400	110000	11000000
12.225		01000001	15.425		11000001
12.250		01000010	15.450		11000010
12.275		01000011	15.475		11000011
12.300	010001	01000100	15.500	110001	11000100
12.325		01000101	15.525		11000101

SetPoint (V)	Code6 (A,D,E)	Code8 (B,C, F)	SetPoint (V)	Code6 (A,D,E)	Code8 (B,C, F)
12.350		01000110	15.550		11000110
12.375		01000111	15.575		11000111
12.400	010010	01001000	15.600	110010	11001000
12.425		01001001	15.625		11001001
12.450		01001010	15.650		11001010
12.475		01001011	15.675		11001011
12.500	010011	01001100	15.700	110011	11001100
12.525		01001101	15.725		11001101
12.550		01001110	15.750		11001110
12.575		01001111	15.775		11001111
12.600	010100	01010000	15.800	110100	11010000
12.625		01010001	15.825		11010001
12.650		01010010	15.850		11010010
12.675		01010011	15.875		11010011
12.700	010101	01010100	15.900	110101	11010100
12.725		01010101	15.925		11010101
12.750		01010110	15.950		11010110
12.775		01010111	15.975		11010111
12.800	010110	01011000	16.000	110110	11011100
12.825		01011001	16.000		11011101
12.850		01011010	16.000		11011110
12.875		01011011	16.000		11011111
12.900	010111	01011100	16.000	110111	11100000
12.925		01011101	16.000		11100001
12.950		01011110	16.000		11100010
12.975		01011111	16.000		11100011
13.000	011000	01100000	16.000	111000	11100100
13.025		01100001	16.000		11100101
13.050		01100010	16.000		11100110
13.075		01100011	16.000		11100111
13.100	011001	01100100	16.000	111001	11100100
13.125		01100101	16.000		11100101
13.150		01100110	16.000		11100110
13.175		01100111	16.000		11100111
13.200	011010	01101000	16.000	111010	11101000
13.225		01101001	16.000		11101001
13.250		01101010	16.000		11101010
13.275		01101011	16.000		11101011
13.300	011011	01101100	16.000	111011	11101100
13.325		01101101	16.000		11101101
13.350		01101110	16.000		11101110

SetPoint (V)	Code6 (A,D,E)	Code8 (B,C, F)	SetPoint (V)	Code6 (A,D,E)	Code8 (B,C, F)
13.375		01101111	16.000		11101111
13.400	011100	01110000	16.000	111100	11110000
13.425		01110001	16.000		11110001
13.450		01110010	16.000		11110010
13.475		01110011	16.000		11110011
13.500	011101	01110100	16.000	111101	11110100
13.525		01110101	16.000		11110101
13.550		01110110	16.000		11110110
13.575		01110111	16.000		11110111
13.600	011110	01111000	16.000	111110	11111000
13.625		01111001	16.000		11111001
13.650		01111010	16.000		11111010
13.675		01111011	16.000		11111011
13.700	011111	01111100	16.000	111111 (1)	11111100
13.725		01111101	16.000		11111101
13.750		01111110	16.000		11111110
13.775		01111111	16.000		11111111 (2)

1. *14.5V @Tj = 25 °C with thermal drift -4mV/°C only for E version*
2. *14.2V @Tj = 25 °C with thermal drift -4.27mV/°C only for C version*

A.3 LRC-Rise tables

Table 41. LRC-rise table

Code	LRC-Rise (s)				
	Default (3 bit)	(B1) Version: A,D	(B2) Version: B, F	(B3) Version: C	(B4) Version: E
0000	1.00	0.00	0.00	0.00	0
0001	2.00	1.00	0.25	0.30	1.3
0010	3.00	2.00	0.50	0.60	2.1
0011	4.00	3.00	0.75	0.90	3
0100	5.00	4.00	1.00	1.30	3.8
0101	6.00	5.00	2.00	1.70	4.7
0110	7.00	6.00	3.00	2.10	5.5
0111	8.00	7.00	4.00	3.00	6.4
1000	-	8.00	5.00	3.90	7.2
1001	-	9.00	6.00	4.80	8.1
1010	-	10.00	7.00	5.70	8.9
1011	-	11.00	8.00	6.60	9.8
1100	-	12.00	9.00	8.40	10.6
1101	-	13.00	10.00	10.20	11.5
1110	-	14.00	12.00	12.60	12.3
1111	-	15.00	15.00	15.00	13.2

A.4 LRC Cut-speed tables

Table 42. **LRC Cut-Speed Tables**

Code	LRC-Cut Speed (RPM)		
	Default (2 bit)	(C1) Version: A,B,D, E, F	(C2) Version: C
0000	3000	2400	1440
0001	4000	2530	1620
0010	4800	2670	1810
0011	6000	2830	2030
0100		3000	2280
0101		3200	2560
0110		3430	2870
0111		3690	3220
1000		4000	3620
1001		4360	4060
1010		4790	4550
1011		5320	5110
1100		5990	5730
1101		6860	6430
1110		8010	7200
1111		Always active	Always active

A.5 Excitation current limitation

Table 43. **D5 – Excitation current limitation 5 bit reference, version A/D**

Code	Exc Current (A)	Code	Exc Current (A)	Code	Exc Current (A)	Code	Exc Current (A)
00000	No limitation	01000	2.0	10000	4.0	11000	6.0
00001	2.0	01001	2.25	10001	4.25	11001	6.25
00010	2.0	01010	2.50	10010	4.50	11010	6.50
00011	2.0	01011	2.75	10011	4.75	11011	6.75
00100	2.0	01100	3.0	10100	5.0	11100	7.0
00101	2.0	01101	3.25	10101	5.25	11101	7.25
00110	2.0	01110	3.50	10110	5.50	11110	7.50
00111	2.0	01111	3.75	10111	5.75	11111	7.75

Table 44. **D7 - Excitation current limitation 7 bit reference, version B/F**

Code	Exc Current (A)	Code	Exc Current (A)	Code	Exc Current (A)	Code	Exc Current (A)
0000000	No limitation	0100000	3.2	1000000	6.4	1100000	9.6
0000001	0.1	0100001	3.3	1000001	6.5	1100001	9.7
0000010	0.2	0100010	3.4	1000010	6.6	1100010	9.8
0000011	0.3	0100011	3.5	1000011	6.7	1100011	9.9

Code	Exc Current (A)	Code	Exc Current (A)	Code	Exc Current (A)	Code	Exc Current (A)
0000100	0.4	0100100	3.6	1000100	6.8	1100100	10.0
0000101	0.5	0100101	3.7	1000101	6.9	1100101	10.1
0000110	0.6	0100110	3.8	1000110	7.0	1100110	10.2
0000111	0.7	0100111	3.9	1000111	7.1	1100111	10.3
0001000	0.8	0101000	4.0	1001000	7.2	1101000	10.4
0001001	0.9	0101001	4.1	1001001	7.3	1101001	10.5
0001010	1.0	0101010	4.2	1001010	7.4	1101010	10.6
0001011	1.1	0101011	4.3	1001011	7.5	1101011	10.7
0001100	1.2	0101100	4.4	1001100	7.6	1101100	10.8
0001101	1.3	0101101	4.5	1001101	7.7	1101101	10.9
0001110	1.4	0101110	4.6	1001110	7.8	1101110	11.0
0001111	1.5	0101111	4.7	1001111	7.9	1101111	11.1
0010000	1.6	0110000	4.8	1010000	8.0	1110000	11.2
0010001	1.7	0110001	4.9	1010001	8.1	1110001	11.3
0010010	1.8	0110010	5.0	1010010	8.2	1110010	11.4
0010011	1.9	0110011	5.1	1010011	8.3	1110011	11.5
0010100	2.0	0110100	5.2	1010100	8.4	1110100	11.6
0010101	2.1	0110101	5.3	1010101	8.5	1110101	11.7
0010110	2.2	0110110	5.4	1010110	8.6	1110110	11.8
0010111	2.3	0110111	5.5	1010111	8.7	1110111	11.9
0011000	2.4	0111000	5.6	1011000	8.8	1111000	12.0
0011001	2.5	0111001	5.7	1011001	8.9	1111001	12.1
0011010	2.6	0111010	5.8	1011010	9.0	1111010	12.2
0011011	2.7	0111011	5.9	1011011	9.1	1111011	12.3
0011100	2.8	0111100	6.0	1011100	9.2	1111100	12.4
0011101	2.9	0111101	6.1	1011101	9.3	1111101	12.5
0011110	3.0	0111110	6.2	1011110	9.4	1111110	12.6
0011111	3.1	0111111	6.3	1011111	9.5	1111111	12.7

Table 45. D8 - Excitation current limitation 8 bit reference, version C

Code	Exc Current (A)	Code	Exc Current (A)	Code	Exc Current (A)	Code	Exc Current (A)
0	Reg. OFF	1000000	2.56	10000000	5.12	11000000	7.68
1	0.04	1000001	2.6	10000001	5.16	11000001	7.72
10	0.08	1000010	2.64	10000010	5.2	11000010	7.76
11	0.12.	1000011	2.68	10000011	5.24	11000011	7.8
100	0.16	1000100	2.72	10000100	5.28	11000100	7.84
101	0.2	1000101	2.76	10000101	5.32	11000101	7.88
110	0.24	1000110	2.8	10000110	5.36	11000110	7.92
111	0.28	1000111	2.84	10000111	5.4	11000111	7.96
1000	0.32	1001000	2.88	10001000	5.44	11001000	8

Code	Exc Current (A)	Code	Exc Current (A)	Code	Exc Current (A)	Code	Exc Current (A)
1001	0.36	1001001	2.92	10001001	5.48	11001001	8
1010	0.4	1001010	2.96	10001010	5.52	11001010	8
1011	0.44	1001011	3	10001011	5.56	11001011	8
1100	0.48	1001100	3.04	10001100	5.6	11001100	8
1101	0.52	1001101	3.08	10001101	5.64	11001101	8
1110	0.56	1001110	3.12	10001110	5.68	11001110	8
1111	0.6	1001111	3.16	10001111	5.72	11001111	8
10000	0.64	1010000	3.2	10010000	5.76	11010000	8
10001	0.68	1010001	3.24	10010001	5.8	11010001	8
10010	0.72	1010010	3.28	10010010	5.84	11010010	8
10011	0.76	1010011	3.32	10010011	5.88	11010011	8
10100	0.8	1010100	3.36	10010100	5.92	11010100	8
10101	0.84	1010101	3.4	10010101	5.96	11010101	8
10110	0.88	1010110	3.44	10010110	6	11010110	8
10111	0.92	1010111	3.48	10010111	6.04	11010111	8
11000	0.96	1011000	3.52	10011000	6.08	11011000	8
11001	1	1011001	3.56	10011001	6.12	11011001	8
11010	1.04	1011010	3.6	10011010	6.16	11011010	8
11011	1.08	1011011	3.64	10011011	6.2	11011011	8
11100	1.12	1011100	3.68	10011100	6.24	11011100	8
11101	1.16	1011101	3.72	10011101	6.28	11011101	8
11110	1.2	1011110	3.76	10011110	6.32	11011110	8
11111	1.24	1011111	3.8	10011111	6.36	11011111	8
100000	1.28	1100000	3.84	10100000	6.4	11100000	8
100001	1.32	1100001	3.88	10100001	6.44	11100001	8
100010	1.36	1100010	3.92	10100010	6.48	11100010	8
100011	1.4	1100011	3.96	10100011	6.52	11100011	8
100100	1.44	1100100	4	10100100	6.56	11100100	8
100101	1.48	1100101	4.04	10100101	6.6	11100101	8
100110	1.52	1100110	4.08	10100110	6.64	11100110	8
100111	1.56	1100111	4.12	10100111	6.68	11100111	8
101000	1.6	1101000	4.16	10101000	6.72	11101000	8
101001	1.64	1101001	4.2	10101001	6.76	11101001	8
101010	1.68	1101010	4.24	10101010	6.8	11101010	8
101011	1.72	1101011	4.28	10101011	6.84	11101011	8
101100	1.76	1101100	4.32	10101100	6.88	11101100	8
101101	1.8	1101101	4.36	10101101	6.92	11101101	8
101110	1.84	1101110	4.4	10101110	6.96	11101110	8
101111	1.88	1101111	4.44	10101111	7	11101111	8
110000	1.92	1110000	4.48	10110000	7.04	11110000	8
110001	1.96	1110001	4.52	10110001	7.08	11110001	8

Code	Exc Current (A)	Code	Exc Current (A)	Code	Exc Current (A)	Code	Exc Current (A)
110010	2	1110010	4.56	10110010	7.12	11110010	8
110011	2.04	1110011	4.6	10110011	7.16	11110011	8
110100	2.08	1110100	4.64	10110100	7.2	11110100	8
110101	2.12	1110101	4.68	10110101	7.24	11110101	8
110110	2.16	1110110	4.72	10110110	7.28	11110110	8
110111	2.2	1110111	4.76	10110111	7.32	11110111	8
111000	2.24	1111000	4.8	10111000	7.36	11111000	8
111001	2.28	1111001	4.84	10111001	7.4	11111001	8
111010	2.32	1111010	4.88	10111010	7.44	11111010	8
111011	2.36	1111011	4.92	10111011	7.48	11111011	8
111100	2.4	1111100	4.96	10111100	7.52	11111100	8
111101	2.44	1111101	5	10111101	7.56	11111101	8
111110	2.48	1111110	5.04	10111110	7.6	11111110	8
111111	2.52	1111111	5.08	10111111	7.64	11111111	No limitation

Table 46. D8 - Excitation current limitation 8 bit reference, version E

Code	Exc Current (A)	Code	Exc Current (A)	Code	Exc Current (A)	Code	Exc Current (A)
0	Reg. OFF	1000000	2.56	10000000	5.12	11000000	7.68
1	0.04	1000001	2.6	10000001	5.16	11000001	7.72
10	0.08	1000010	2.64	10000010	5.2	11000010	7.76
11	0.12	1000011	2.68	10000011	5.24	11000011	7.8
100	0.16	1000100	2.72	10000100	5.28	11000100	7.84
101	0.2	1000101	2.76	10000101	5.32	11000101	7.88
110	0.24	1000110	2.8	10000110	5.36	11000110	7.92
111	0.28	1000111	2.84	10000111	5.4	11000111	7.96
1000	0.32	1001000	2.88	10001000	5.44	11001000	8
1001	0.36	1001001	2.92	10001001	5.48	11001001	8.04
1010	0.4	1001010	2.96	10001010	5.52	11001010	8.08
1011	0.44	1001011	3	10001011	5.56	11001011	8.12
1100	0.48	1001100	3.04	10001100	5.6	11001100	8.16
1101	0.52	1001101	3.08	10001101	5.64	11001101	8.2
1110	0.56	1001110	3.12	10001110	5.68	11001110	8.24
1111	0.6	1001111	3.16	10001111	5.72	11001111	8.28
10000	0.64	1010000	3.2	10010000	5.76	11010000	8.32
10001	0.68	1010001	3.24	10010001	5.8	11010001	8.36
10010	0.72	1010010	3.28	10010010	5.84	11010010	8.4
10011	0.76	1010011	3.32	10010011	5.88	11010011	8.44
10100	0.8	1010100	3.36	10010100	5.92	11010100	8.48
10101	0.84	1010101	3.4	10010101	5.96	11010101	8.52
10110	0.88	1010110	3.44	10010110	6	11010110	8.56

Code	Exc Current (A)	Code	Exc Current (A)	Code	Exc Current (A)	Code	Exc Current (A)
10111	0.92	1010111	3.48	10010111	6.04	11010111	8.6
11000	0.96	1011000	3.52	10011000	6.08	11011000	8.64
11001	1	1011001	3.56	10011001	6.12	11011001	8.68
11010	1.04	1011010	3.6	10011010	6.16	11011010	8.72
11011	1.08	1011011	3.64	10011011	6.2	11011011	8.76
11100	1.12	1011100	3.68	10011100	6.24	11011100	8.8
11101	1.16	1011101	3.72	10011101	6.28	11011101	8.84
11110	1.2	1011110	3.76	10011110	6.32	11011110	8.88
11111	1.24	1011111	3.8	10011111	6.36	11011111	8.92
100000	1.28	1100000	3.84	10100000	6.4	11100000	8.96
100001	1.32	1100001	3.88	10100001	6.44	11100001	9
100010	1.36	1100010	3.92	10100010	6.48	11100010	9.04
100011	1.4	1100011	3.96	10100011	6.52	11100011	9.08
100100	1.44	1100100	4	10100100	6.56	11100100	9.12
100101	1.48	1100101	4.04	10100101	6.6	11100101	9.16
100110	1.52	1100110	4.08	10100110	6.64	11100110	9.2
100111	1.56	1100111	4.12	10100111	6.68	11100111	9.24
101000	1.6	1101000	4.16	10101000	6.72	11101000	9.28
101001	1.64	1101001	4.2	10101001	6.76	11101001	9.32
101010	1.68	1101010	4.24	10101010	6.8	11101010	9.36
101011	1.72	1101011	4.28	10101011	6.84	11101011	9.4
101100	1.76	1101100	4.32	10101100	6.88	11101100	9.44
101101	1.8	1101101	4.36	10101101	6.92	11101101	9.48
101110	1.84	1101110	4.4	10101110	6.96	11101110	9.52
101111	1.88	1101111	4.44	10101111	7	11101111	9.56
110000	1.92	1110000	4.48	10110000	7.04	11110000	9.6
110001	1.96	1110001	4.52	10110001	7.08	11110001	9.64
110010	2	1110010	4.56	10110010	7.12	11110010	9.68
110011	2.04	1110011	4.6	10110011	7.16	11110011	9.72
110100	2.08	1110100	4.64	10110100	7.2	11110100	9.76
110101	2.12	1110101	4.68	10110101	7.24	11110101	9.8
110110	2.16	1110110	4.72	10110110	7.28	11110110	9.84
110111	2.2	1110111	4.76	10110111	7.32	11110111	9.88
111000	2.24	1111000	4.8	10111000	7.36	11111000	9.92
111001	2.28	1111001	4.84	10111001	7.4	11111001	9.96
111010	2.32	1111010	4.88	10111010	7.44	11111010	10
111011	2.36	1111011	4.92	10111011	7.48	11111011	10.04
111100	2.4	1111100	4.96	10111100	7.52	11111100	10.08
111101	2.44	1111101	5	10111101	7.56	11111101	10.12
111110	2.48	1111110	5.04	10111110	7.6	11111110	10.16
111111	2.52	1111111	5.08	10111111	7.64	11111111	No limitation

A.6 Blind zone

Table 47. **BZ - blind zone values, 1 bit reference version A, B, E, F**

Code	BZ
0	3%
1	12%

Table 48. **Blind zone values, 2 bits reference version C**

Code	BZ
00	0
01	3.125%
10	6.25%
11	12.5%

A.7 Voltage limitation for high temperatures

Table 49. **SetPoint limitation threshold for high temperature (delta), 3 bits reference version A, B**

Code	Temperature
000	Default value 0 °C
001	Default value –16 °C
010	Default value –12 °C
011	Default value –8 °C
100	Default value –4 °C
101	Default value +4 °C
110	Default value +8 °C
111	Default value +12 °C

A.8 Excitation duty cycle value

Table 50. **DCE5 – Duty cycle value, 5 bits reference version A, B, D, E, F**

Code	Duty Cycle (%)	Code	Duty Cycle (%)
00000	0 < DF < 3.125	10000	50 < DF < 53.125
00001	3.125 < DF < 6.25	10001	53.125 < DF < 56.25
00010	6.25 < DF < 9.375	10010	56.25 < DF < 59.375
00011	9.375 < DF < 12.5	10011	59.375 < DF < 62.5
00100	12.5 < DF < 15.625	10100	62.5 < DF < 65.625
00101	15.625 < DF < 18.75	10101	65.625 < DF < 68.75
00110	18.75 < DF < 21.875	10110	68.75 < DF < 71.875
00111	21.875 < DF < 25	10111	71.875 < DF < 75
01000	25 < DF < 28.125	11000	75 < DF < 78.125
01001	28.125 < DF <	11001	78.125 < DF < 81.25

Code	Duty Cycle (%)	Code	Duty Cycle (%)
01010	31.25 < DF < 34.375	11010	81.25 < DF < 84.375
01011	34.375 < DF < 37.5	11011	84.375 < DF < 87.5
01100	37.5 < DF < 40.625	11100	87.5 < DF < 90.625
01101	40.625 < DF <	11101	90.625 < DF < 93.75
01110	43.75 < DF < 46.875	11110	93.75 < DF < 96.875
01111	46.875 < DF < 50	11111	96.875 < DF < 100

Table 51. DCE8 – Duty cycle value, 8 bits reference version C

Code	Duty Cycle (%)	Code	Duty Cycle (%)	Code	Duty Cycle (%)	Code	Duty Cycle (%)
00000000	0.39	01000000	25.39	10000000	50.39	11000000	75.39
00000001	0.78	01000001	25.78	10000001	50.78	11000001	75.78
00000010	1.17	01000010	26.17	10000010	51.17	10000010	76.17
00000011	1.56	01000011	26.56	10000011	51.56	10000011	76.56
00000100	1.95	01000100	26.95	10000100	51.95	11000100	76.95
00000101	2.34	01000101	27.34	10000101	52.34	11000101	77.34
00000110	2.73	01000110	27.73	10000110	52.73	11000110	77.73
00000111	3.13	01000111	28.13	10000111	53.13	11000111	78.13
00001000	3.52	01001000	28.52	10001000	53.52	11001000	78.52
00001001	3.91	01001001	28.91	10001001	53.91	11001001	78.91
00001010	4.30	01001010	29.30	10001010	54.30	11001010	79.30
00001011	4.69	01001011	29.69	10001011	54.69	11001011	79.69
00001100	5.08	01001100	30.08	10001100	55.08	11001100	80.08
00001101	5.47	01001101	30.47	10001101	55.47	11001101	80.47
00001110	5.86	01001110	30.86	10001110	55.86	11001110	80.86
00001111	6.25	01001111	31.25	10001111	56.25	11001111	81.25
00010000	6.64	01010000	31.64	10010000	56.64	11010000	81.64
00010001	7.03	01010001	32.03	10010001	57.03	11010001	82.03
00010010	7.42	01010010	32.42	10010010	57.42	11010010	82.42
00010011	7.81	01010011	32.81	10010011	57.81	11010011	82.81
00010100	8.20	01010100	33.20	10010100	58.20	11010100	83.20
00010101	8.59	01010101	33.59	10010101	58.59	11010101	83.59
00010110	8.98	01010110	33.98	10010110	58.98	11010110	83.98
00010111	9.38	01010111	34.38	10010111	59.38	11010111	84.38
00011000	9.77	01011000	34.77	10011000	59.77	11011100	84.77
00011001	10.16	01011001	35.16	10011001	60.16	10011101	85.16
00011010	10.55	01011010	35.55	10011010	60.55	10011110	85.55
00011011	10.94	01011011	35.94	10011011	60.94	10011111	85.94
00011100	11.33	01011100	36.33	10011100	61.33	11100000	86.33
00011101	11.72	01011101	36.72	10011101	61.72	11100001	86.72
00011110	12.11	01011110	37.11	10011110	62.11	11100010	87.11

Code	Duty Cycle (%)	Code	Duty Cycle (%)	Code	Duty Cycle (%)	Code	Duty Cycle (%)
00011111	12.50	01011111	37.50	10011111	62.50	11100011	87.50
00100000	12.89	01100000	37.89	10100000	62.89	11100100	87.89
00100001	13.28	01100001	38.28	10100001	63.28	11100101	88.28
00100010	13.67	01100010	38.67	10100010	63.67	11100110	88.67
00100011	14.06	01100011	39.06	10100011	64.06	11100111	89.06
00100100	14.45	01100100	39.45	10100100	64.45	11100100	89.45
00100101	14.84	01100101	39.84	10100101	64.84	11100101	89.84
00100110	15.23	01100110	40.23	10100110	65.23	11100110	90.23
00100111	15.63	01100111	40.63	10100111	65.63	11100111	90.63
00101000	16.02	01101000	41.02	10101000	66.02	11101000	91.02
00101001	16.41	01101001	41.41	10101001	66.41	11101001	91.41
00101010	16.80	01101010	41.80	10101010	66.80	11101010	91.80
00101011	17.19	01101011	42.19	10101011	67.19	11101011	92.19
00101100	17.58	01101100	42.58	10101100	67.58	11101100	92.58
00101101	17.97	01101101	42.97	10101101	67.97	11101101	92.97
00101110	18.36	01101110	43.36	10101110	68.36	11101110	93.36
00101111	18.75	01101111	43.75	10101111	68.75	11101111	93.75
00110000	19.14	01110000	44.14	10110000	69.14	11110000	94.14
00110001	19.53	01110001	44.53	10110001	69.53	11110001	94.53
00110010	19.92	01110010	44.92	10110010	69.92	11110010	94.92
00110011	20.31	01110011	45.31	10110011	70.31	11110011	95.31
00110100	20.70	01110100	45.70	10110100	70.70	11110100	95.70
00110101	21.09	01110101	46.09	10110101	71.09	11110101	96.09
00110110	21.48	01110110	46.48	10110110	71.48	11110110	96.48
00110111	21.88	01110111	46.88	10110111	71.88	11110111	96.88
00111000	22.27	01111000	47.27	10111000	72.27	11111000	97.27
00111001	22.66	01111001	47.66	10111001	72.66	11111001	97.66
00111010	23.05	01111010	48.05	10111010	73.05	11111010	98.05
00111011	23.44	01111011	48.44	10111011	73.44	11111011	98.44
00111100	23.83	01111100	48.83	10111100	73.83	11111100	98.83
00111101	24.22	01111101	49.22	10111101	74.22	11111101	99.22
00111110	24.61	01111110	49.61	10111110	74.61	11111110	99.61
00111111	25.00	01111111	50.00	10111111	75.00	11111111	100.00

A.9 Excitation current measure

Table 52. EXC6 - Excitation current measure 6 bit reference, Version A and D (with Iexc)

Code	Exc Curr. Measure (A)	Code	Exc Curr. Measure (A)	Code	Exc Curr. Measure (A)	Code	Exc Curr. Measure (A)
000000	0	010000	2	100000	4	110000	6
000001	0.125	010001	2.125	100001	4.125	110001	6.125

Code	Exc Curr. Measure (A)	Code	Exc Curr. Measure (A)	Code	Exc Curr. Measure (A)	Code	Exc Curr. Measure (A)
000010	0.25	010010	2.25	100010	4.25	110010	6.25
000011	0.375	010011	2.375	100011	4.375	110011	6.375
000100	0.5	010100	2.5	100100	4.5	110100	6.5
000101	0.625	010101	2.625	100101	4.625	110101	6.625
000110	0.75	010110	2.75	100110	4.75	110110	6.75
000111	0.875	010111	2.875	100111	4.875	110111	6.875
001000	1	011000	3	101000	5	111000	7
001001	1.125	011001	3.125	101001	5.125	111001	7.125
001010	1.25	011010	3.25	101010	5.25	111010	7.25
001011	1.375	011011	3.375	101011	5.375	111011	7.375
001100	1.5	011100	3.5	101100	5.5	111100	7.5
001101	1.625	011101	3.625	101101	5.625	111101	7.625
001110	1.75	011110	3.75	101110	5.75	111110	7.75
001111	1.875	011111	3.875	101111	5.875	111111	≥7.875

Table 53. EXC8 - Excitation current measure 8 bit reference version A and B

Code	Exc Curr. Measure (A)	Code	Exc Curr. Measure (A)	Code	Exc Curr. Measure (A)	Code	Exc Curr. Measure (A)
00000000	0.00	01000000	3.20	10000000	6.40	11000000	9.60
00000001	0.05	01000001	3.25	10000001	6.45	11000001	9.65
00000010	0.10	01000010	3.30	10000010	6.50	11000010	9.70
00000011	0.15	01000011	3.35	10000011	6.55	11000011	9.75
00000100	0.20	01000100	3.40	10000100	6.60	11000100	9.80
00000101	0.25	01000101	3.45	10000101	6.65	11000101	9.85
00000110	0.30	01000110	3.50	10000110	6.70	11000110	9.90
00000111	0.35	01000111	3.55	10000111	6.75	11000111	9.95
00001000	0.40	01001000	3.60	10001000	6.80	11001000	10.00
00001001	0.45	01001001	3.65	10001001	6.85	11001001	10.05
00001010	0.50	01001010	3.70	10001010	6.90	11001010	10.10
00001011	0.55	01001011	3.75	10001011	6.95	11001011	10.15
00001100	0.60	01001100	3.80	10001100	7.00	11001100	10.20
00001101	0.65	01001101	3.85	10001101	7.05	11001101	10.25
00001110	0.70	01001110	3.90	10001110	7.10	11001110	10.30
00001111	0.75	01001111	3.95	10001111	7.15	11001111	10.35
00010000	0.80	01010000	4.00	10010000	7.20	11010000	10.40
00010001	0.85	01010001	4.05	10010001	7.25	11010001	10.45
00010010	0.90	01010010	4.10	10010010	7.30	11010010	10.50
00010011	0.95	01010011	4.15	10010011	7.35	11010011	10.55
00010100	1.00	01010100	4.20	10010100	7.40	11010100	10.60
00010101	1.05	01010101	4.25	10010101	7.45	11010101	10.65

Code	Exc Curr. Measure (A)	Code	Exc Curr. Measure (A)	Code	Exc Curr. Measure (A)	Code	Exc Curr. Measure (A)
00010110	1.10	01010110	4.30	10010110	7.50	11010110	10.70
00010111	1.15	01010111	4.35	10010111	7.55	11010111	10.75
00011000	1.20	01011000	4.40	10011000	7.60	11011000	10.80
00011001	1.25	01011001	4.45	10011001	7.65	11011001	10.85
00011010	1.30	01011010	4.50	10011010	7.70	11011010	10.90
00011011	1.35	01011011	4.55	10011011	7.75	11011011	10.95
00011100	1.40	01011100	4.60	10011100	7.80	11011100	11.00
00011101	1.45	01011101	4.65	10011101	7.85	11011101	11.05
00011110	1.50	01011110	4.70	10011110	7.90	11011110	11.10
00011111	1.55	01011111	4.75	10011111	7.95	11011111	11.15
00100000	1.60	01100000	4.80	10100000	8.00	11100000	11.20
00100001	1.65	01100001	4.85	10100001	8.05	11100001	11.25
00100010	1.70	01100010	4.90	10100010	8.10	11100010	11.30
00100011	1.75	01100011	4.95	10100011	8.15	11100011	11.35
00100100	1.80	01100100	5.00	10100100	8.20	11100100	11.40
00100101	1.85	01100101	5.05	10100101	8.25	11100101	11.45
00100110	1.90	01100110	5.10	10100110	8.30	11100110	11.50
00100111	1.95	01100111	5.15	10100111	8.35	11100111	11.55
00101000	2.00	01101000	5.20	10101000	8.40	11101000	11.60
00101001	2.05	01101001	5.25	10101001	8.45	11101001	11.65
00101010	2.10	01101010	5.30	10101010	8.50	11101010	11.70
00101011	2.15	01101011	5.35	10101011	8.55	11101011	11.75
00101100	2.20	01101100	5.40	10101100	8.60	11101100	11.80
00101101	2.25	01101101	5.45	10101101	8.65	11101101	11.85
00101110	2.30	01101110	5.50	10101110	8.70	11101110	11.90
00101111	2.35	01101111	5.55	10101111	8.75	11101111	11.95
00110000	2.40	01110000	5.60	10110000	8.80	11110000	12.00
00110001	2.45	01110001	5.65	10110001	8.85	11110001	12.05
00110010	2.50	01110010	5.70	10110010	8.90	11110010	12.10
00110011	2.55	01110011	5.75	10110011	8.95	11110011	12.15
00110100	2.60	01110100	5.80	10110100	9.00	11110100	12.20
00110101	2.65	01110101	5.85	10110101	9.05	11110101	12.25
00110110	2.70	01110110	5.90	10110110	9.10	11110110	12.30
00110111	2.75	01110111	5.95	10110111	9.15	11110111	12.35
00111000	2.80	01111000	6.00	10111000	9.20	11111000	12.40
00111001	2.85	01111001	6.05	10111001	9.25	11111001	12.45
00111010	2.90	01111010	6.10	10111010	9.30	11111010	12.50
00111011	2.95	01111011	6.15	10111011	9.35	11111011	12.55
00111100	3.00	01111100	6.20	10111100	9.40	11111100	12.60
00111101	3.05	01111101	6.25	10111101	9.45	11111101	12.65

Code	Exc Curr. Measure (A)	Code	Exc Curr. Measure (A)	Code	Exc Curr. Measure (A)	Code	Exc Curr. Measure (A)
00111110	3.10	01111110	6.30	10111110	9.50	11111110	12.70
00111111	3.15	01111111	6.35	10111111	9.55	11111111	12.75

Table 54. EXC8 - Excitation current measure 8 bit reference version C

Code	Exc Curr. Measure (A)	Code	Exc Curr. Measure (A)	Code	Exc Curr. Measure (A)	Code	Exc Curr. Measure (A)
00000000	0	01000000	2.56	10000000	5.12	11000000	7.68
00000001	0.04	01000001	2.6	10000001	5.16	11000001	7.72
00000010	0.08	01000010	2.64	10000010	5.2	11000010	7.76
00000011	0.12	01000011	2.68	10000011	5.24	11000011	7.8
00000100	0.16	01000100	2.72	10000100	5.28	11000100	7.84
00000101	0.2	01000101	2.76	10000101	5.32	11000101	7.88
00000110	0.24	01000110	2.8	10000110	5.36	11000110	7.92
00000111	0.28	01000111	2.84	10000111	5.4	11000111	7.96
00001000	0.32	01001000	2.88	10001000	5.44	11001000	8
00001001	0.36	01001001	2.92	10001001	5.48	11001001	8
00001010	0.4	01001010	2.96	10001010	5.52	11001010	8
00001011	0.44	01001011	3	10001011	5.56	11001011	8
00001100	0.48	01001100	3.04	10001100	5.6	11001100	8
00001101	0.52	01001101	3.08	10001101	5.64	11001101	8
00001110	0.56	01001110	3.12	10001110	5.68	11001110	8
00001111	0.6	01001111	3.16	10001111	5.72	11001111	8
00010000	0.64	01010000	3.2	10010000	5.76	11010000	8
00010001	0.68	01010001	3.24	10010001	5.8	11010001	8
00010010	0.72	01010010	3.28	10010010	5.84	11010010	8
00010011	0.76	01010011	3.32	10010011	5.88	11010011	8
00010100	0.8	01010100	3.36	10010100	5.92	11010100	8
00010101	0.84	01010101	3.4	10010101	5.96	11010101	8
00010110	0.88	01010110	3.44	10010110	6	11010110	8
00010111	0.92	01010111	3.48	10010111	6.04	11010111	8
00011000	0.96	01011000	3.52	10011000	6.08	11011000	8
00011001	1	01011001	3.56	10011001	6.12	11011001	8
00011010	1.04	01011010	3.6	10011010	6.16	11011010	8
00011011	1.08	01011011	3.64	10011011	6.2	11011011	8
00011100	1.12	01011100	3.68	10011100	6.24	11011100	8
00011101	1.16	01011101	3.72	10011101	6.28	11011101	8
00011110	1.2	01011110	3.76	10011110	6.32	11011110	8
00011111	1.24	01011111	3.8	10011111	6.36	11011111	8
00100000	1.28	01100000	3.84	10100000	6.4	11100000	8
00100001	1.32	01100001	3.88	10100001	6.44	11100001	8

Code	Exc Curr. Measure (A)	Code	Exc Curr. Measure (A)	Code	Exc Curr. Measure (A)	Code	Exc Curr. Measure (A)
00100010	1.36	01100010	3.92	10100010	6.48	11100010	8
00100011	1.4	01100011	3.96	10100011	6.52	11100011	8
00100100	1.44	01100100	4	10100100	6.56	11100100	8
00100101	1.48	01100101	4.04	10100101	6.6	11100101	8
00100110	1.52	01100110	4.08	10100110	6.64	11100110	8
00100111	1.56	01100111	4.12	10100111	6.68	11100111	8
00101000	1.6	01101000	4.16	10101000	6.72	11101000	8
00101001	1.64	01101001	4.2	10101001	6.76	11101001	8
00101010	1.68	01101010	4.24	10101010	6.8	11101010	8
00101011	1.72	01101011	4.28	10101011	6.84	11101011	8
00101100	1.76	01101100	4.32	10101100	6.88	11101100	8
00101101	1.8	01101101	4.36	10101101	6.92	11101101	8
00101110	1.84	01101110	4.4	10101110	6.96	11101110	8
00101111	1.88	01101111	4.44	10101111	7	11101111	8
00110000	1.92	01110000	4.48	10110000	7.04	11110000	8
00110001	1.96	01110001	4.52	10110001	7.08	11110001	8
00110010	2	01110010	4.56	10110010	7.12	11110010	8
00110011	2.04	01110011	4.6	10110011	7.16	11110011	8
00110100	2.08	01110100	4.64	10110100	7.2	11110100	8
00110101	2.12	01110101	4.68	10110101	7.24	11110101	8
00110110	2.16	01110110	4.72	10110110	7.28	11110110	8
00110111	2.2	01110111	4.76	10110111	7.32	11110111	8
00111000	2.24	01111000	4.8	10111000	7.36	11111000	8
00111001	2.28	01111001	4.84	10111001	7.4	11111001	8
00111010	2.32	01111010	4.88	10111010	7.44	11111010	8
00111011	2.36	01111011	4.92	10111011	7.48	11111011	8
00111100	2.4	01111100	4.96	10111100	7.52	11111100	8
00111101	2.44	01111101	5	10111101	7.56	11111101	8
00111110	2.48	01111110	5.04	10111110	7.6	11111110	8
00111111	2.52	01111111	5.08	10111111	7.64	11111111	8

Table 55. EXC8 - Excitation current measure 8 bit reference version E

Code	Exc Curr. Measure (A)	Code	Exc Curr. Measure (A)	Code	Exc Curr. Measure (A)	Code	Exc Curr. Measure (A)
00000000	0	01000000	2.56	10000000	5.12	11000000	7.68
00000001	0.04	01000001	2.6	10000001	5.16	11000001	7.72
00000010	0.08	01000010	2.64	10000010	5.2	11000010	7.76
00000011	0.12	01000011	2.68	10000011	5.24	11000011	7.8
00000100	0.16	01000100	2.72	10000100	5.28	11000100	7.84
00000101	0.2	01000101	2.76	10000101	5.32	11000101	7.88

Code	Exc Curr. Measure (A)	Code	Exc Curr. Measure (A)	Code	Exc Curr. Measure (A)	Code	Exc Curr. Measure (A)
00000110	0.24	01000110	2.8	10000110	5.36	11000110	7.92
00000111	0.28	01000111	2.84	10000111	5.4	11000111	7.96
00001000	0.32	01001000	2.88	10001000	5.44	11001000	8
00001001	0.36	01001001	2.92	10001001	5.48	11001001	8.04
00001010	0.4	01001010	2.96	10001010	5.52	11001010	8.08
00001011	0.44	01001011	3	10001011	5.56	11001011	8.12
00001100	0.48	01001100	3.04	10001100	5.6	11001100	8.16
00001101	0.52	01001101	3.08	10001101	5.64	11001101	8.2
00001110	0.56	01001110	3.12	10001110	5.68	11001110	8.24
00001111	0.6	01001111	3.16	10001111	5.72	11001111	8.28
00010000	0.64	01010000	3.2	10010000	5.76	11010000	8.32
00010001	0.68	01010001	3.24	10010001	5.8	11010001	8.36
00010010	0.72	01010010	3.28	10010010	5.84	11010010	8.4
00010011	0.76	01010011	3.32	10010011	5.88	11010011	8.44
00010100	0.8	01010100	3.36	10010100	5.92	11010100	8.48
00010101	0.84	01010101	3.4	10010101	5.96	11010101	8.52
00010110	0.88	01010110	3.44	10010110	6	11010110	8.56
00010111	0.92	01010111	3.48	10010111	6.04	11010111	8.6
00011000	0.96	01011000	3.52	10011000	6.08	11011000	8.64
00011001	1	01011001	3.56	10011001	6.12	11011001	8.68
00011010	1.04	01011010	3.6	10011010	6.16	11011010	8.72
00011011	1.08	01011011	3.64	10011011	6.2	11011011	8.76
00011100	1.12	01011100	3.68	10011100	6.24	11011100	8.8
00011101	1.16	01011101	3.72	10011101	6.28	11011101	8.84
00011110	1.2	01011110	3.76	10011110	6.32	11011110	8.88
00011111	1.24	01011111	3.8	10011111	6.36	11011111	8.92
00100000	1.28	01100000	3.84	10100000	6.4	11100000	8.96
00100001	1.32	01100001	3.88	10100001	6.44	11100001	9
00100010	1.36	01100010	3.92	10100010	6.48	11100010	9.04
00100011	1.4	01100011	3.96	10100011	6.52	11100011	9.08
00100100	1.44	01100100	4	10100100	6.56	11100100	9.12
00100101	1.48	01100101	4.04	10100101	6.6	11100101	9.16
00100110	1.52	01100110	4.08	10100110	6.64	11100110	9.2
00100111	1.56	01100111	4.12	10100111	6.68	11100111	9.24
00101000	1.6	01101000	4.16	10101000	6.72	11101000	9.28
00101001	1.64	01101001	4.2	10101001	6.76	11101001	9.32
00101010	1.68	01101010	4.24	10101010	6.8	11101010	9.36
00101011	1.72	01101011	4.28	10101011	6.84	11101011	9.4
00101100	1.76	01101100	4.32	10101100	6.88	11101100	9.44
00101101	1.8	01101101	4.36	10101101	6.92	11101101	9.48

Code	Exc Curr. Measure (A)	Code	Exc Curr. Measure (A)	Code	Exc Curr. Measure (A)	Code	Exc Curr. Measure (A)
00101110	1.84	01101110	4.4	10101110	6.96	11101110	9.52
00101111	1.88	01101111	4.44	10101111	7	11101111	9.56
00110000	1.92	01110000	4.48	10110000	7.04	11110000	9.6
00110001	1.96	01110001	4.52	10110001	7.08	11110001	9.64
00110010	2	01110010	4.56	10110010	7.12	11110010	9.68
00110011	2.04	01110011	4.6	10110011	7.16	11110011	9.72
00110100	2.08	01110100	4.64	10110100	7.2	11110100	9.76
00110101	2.12	01110101	4.68	10110101	7.24	11110101	9.8
00110110	2.16	01110110	4.72	10110110	7.28	11110110	9.84
00110111	2.2	01110111	4.76	10110111	7.32	11110111	9.88
00111000	2.24	01111000	4.8	10111000	7.36	11111000	9.92
00111001	2.28	01111001	4.84	10111001	7.4	11111001	9.96
00111010	2.32	01111010	4.88	10111010	7.44	11111010	10
00111011	2.36	01111011	4.92	10111011	7.48	11111011	10.04
00111100	2.4	01111100	4.96	10111100	7.52	11111100	10.08
00111101	2.44	01111101	5	10111101	7.56	11111101	10.12
00111110	2.48	01111110	5.04	10111110	7.6	11111110	10.16
00111111	2.52	01111111	5.08	10111111	7.64	11111111	10.2

A.10 Battery voltage measure

Table 56. **BV8 – Battery Voltage 8 bit reference version A and B**

Code	BV (V)	Code	BV (V)	Code	BV (V)	Code	BV (V)
00000000	≤8	01000000	14.4	10000000	20.8	11000000	-
00000001	8.1	01000001	14.5	10000001	20.9	11000001	-
00000010	8.2	01000010	14.6	10000010	21	11000010	-
00000011	8.3	01000011	14.7	10000011	21.1	11000011	-
00000100	8.4	01000100	14.8	10000100	21.2	11000100	-
00000101	8.5	01000101	14.9	10000101	21.3	11000101	-
00000110	8.6	01000110	15	10000110	21.4	11000110	-
00000111	8.7	01000111	15.1	10000111	21.5	11000111	-
00001000	8.8	01001000	15.2	10001000	21.6	11001000	-
00001001	8.9	01001001	15.3	10001001	21.7	11001001	-
00001010	9	01001010	15.4	10001010	21.8	11001010	-
00001011	9.1	01001011	15.5	10001011	21.9	11001011	-
00001100	9.2	01001100	15.6	10001100	22	11001100	-
00001101	9.3	01001101	15.7	10001101	22.1	11001101	-
00001110	9.4	01001110	15.8	10001110	22.2	11001110	-
00001111	9.5	01001111	15.9	10001111	22.3	11001111	-
00010000	9.6	01010000	16	10010000	22.4	11010000	-

Code	BV (V)	Code	BV (V)	Code	BV (V)	Code	BV (V)
00010001	9.7	01010001	16.1	10010001	22.5	11010001	-
00010010	9.8	01010010	16.2	10010010	22.6	11010010	-
00010011	9.9	01010011	16.3	10010011	22.7	11010011	-
00010100	10	01010100	16.4	10010100	22.8	11010100	-
00010101	10.1	01010101	16.5	10010101	22.9	11010101	-
00010110	10.2	01010110	16.6	10010110	23	11010110	-
00010111	10.3	01010111	16.7	10010111	23.1	11010111	-
00011000	10.4	01011000	16.8	10011000	23.2	11011000	-
00011001	10.5	01011001	16.9	10011001	23.3	11011001	-
00011010	10.6	01011010	17	10011010	23.4	11011010	-
00011011	10.7	01011011	17.1	10011011	23.5	11011011	-
00011100	10.8	01011100	17.2	10011100	23.6	11011100	-
00011101	10.9	01011101	17.3	10011101	23.7	11011101	-
00011110	11	01011110	17.4	10011110	23.8	11011110	-
00011111	11.1	01011111	17.5	10011111	23.9	11011111	-
00100000	11.2	01100000	17.6	10100000	≥24	11100000	-
00100001	11.3	01100001	17.7	10100001	-	11100001	-
00100010	11.4	01100010	17.8	10100010	-	11100010	-
00100011	11.5	01100011	17.9	10100011	-	11100011	-
00100100	11.6	01100100	18	10100100	-	11100100	-
00100101	11.7	01100101	18.1	10100101	-	11100101	-
00100110	11.8	01100110	18.2	10100110	-	11100110	-
00100111	11.9	01100111	18.3	10100111	-	11100111	-
00101000	12	01101000	18.4	10101000	-	11101000	-
00101001	12.1	01101001	18.5	10101001	-	11101001	-
00101010	12.2	01101010	18.6	10101010	-	11101010	-
00101011	12.3	01101011	18.7	10101011	-	11101011	-
00101100	12.4	01101100	18.8	10101100	-	11101100	-
00101101	12.5	01101101	18.9	10101101	-	11101101	-
00101110	12.6	01101110	19	10101110	-	11101110	-
00101111	12.7	01101111	19.1	10101111	-	11101111	-
00110000	12.8	01110000	19.2	10110000	-	11110000	-
00110001	12.9	01110001	19.3	10110001	-	11110001	-
00110010	13	01110010	19.4	10110010	-	11110010	-
00110011	13.1	01110011	19.5	10110011	-	11110011	-
00110100	13.2	01110100	19.6	10110100	-	11110100	-
00110101	13.3	01110101	19.7	10110101	-	11110101	-
00110110	13.4	01110110	19.8	10110110	-	11110110	-
00110111	13.5	01110111	19.9	10110111	-	11110111	-
00111000	13.6	01111000	20	10111000	-	11111000	-
00111001	13.7	01111001	20.1	10111001	-	11111001	-

Code	BV (V)	Code	BV (V)	Code	BV (V)	Code	BV (V)
00111010	13.8	01111010	20.2	10111010	-	11111010	-
00111011	13.9	01111011	20.3	10111011	-	11111011	-
00111100	14	01111100	20.4	10111100	-	11111100	-
00111101	14.1	01111101	20.5	10111101	-	11111101	-
00111110	14.2	01111110	20.6	10111110	-	11111110	-
00111111	14.3	01111111	20.7	10111111	-	11111111	-

Table 57. BV8C – Battery Voltage 8 bit reference version C

Code	BV (V)	Code	BV (V)	Code	BV (V)	Code	BV (V)
00000000	9.00	01000000	12.20	10000000	15.40	11000000	18.00
00000001	9.05	01000001	12.25	10000001	15.45	11000001	18.00
00000010	9.10	01000010	12.30	10000010	15.50	11000010	18.00
00000011	9.15	01000011	12.35	10000011	15.55	11000011	18.00
00000100	9.20	01000100	12.40	10000100	15.60	11000100	18.00
00000101	9.25	01000101	12.45	10000101	15.65	11000101	18.00
00000110	9.30	01000110	12.50	10000110	15.70	11000110	18.00
00000111	9.35	01000111	12.55	10000111	15.75	11000111	18.00
00001000	9.40	01001000	12.60	10001000	15.80	11001000	18.00
00001001	9.45	01001001	12.65	10001001	15.85	11001001	18.00
00001010	9.50	01001010	12.70	10001010	15.90	11001010	18.00
00001011	9.55	01001011	12.75	10001011	15.95	11001011	18.00
00001100	9.60	01001100	12.80	10001100	16.00	11001100	18.00
00001101	9.65	01001101	12.85	10001101	16.05	11001101	18.00
00001110	9.70	01001110	12.90	10001110	16.10	11001110	18.00
00001111	9.75	01001111	12.95	10001111	16.15	11001111	18.00
00010000	9.80	01010000	13.00	10010000	16.20	11010000	18.00
00010001	9.85	01010001	13.05	10010001	16.25	11010001	18.00
00010010	9.90	01010010	13.10	10010010	16.30	11010010	18.00
00010011	9.95	01010011	13.15	10010011	16.35	11010011	18.00
00010100	10.00	01010100	13.20	10010100	16.40	11010100	18.00
00010101	10.05	01010101	13.25	10010101	16.45	11010101	18.00
00010110	10.10	01010110	13.30	10010110	16.50	11010110	18.00
00010111	10.15	01010111	13.35	10010111	16.55	11010111	18.00
00011000	10.20	01011000	13.40	10011000	16.60	11011000	18.00
00011001	10.25	01011001	13.45	10011001	16.65	11011001	18.00
00011010	10.30	01011010	13.50	10011010	16.70	11011010	18.00
00011011	10.35	01011011	13.55	10011011	16.75	11011011	18.00
00011100	10.40	01011100	13.60	10011100	16.80	11011100	18.00
00011101	10.45	01011101	13.65	10011101	16.85	11011101	18.00
00011110	10.50	01011110	13.70	10011110	16.90	11011110	18.00

Code	BV (V)	Code	BV (V)	Code	BV (V)	Code	BV (V)
00011111	10.55	01011111	13.75	10011111	16.95	11011111	18.00
00100000	10.60	01100000	13.80	10100000	17.00	11100000	18.00
00100001	10.65	01100001	13.85	10100001	17.05	11100001	18.00
00100010	10.70	01100010	13.90	10100010	17.10	11100010	18.00
00100011	10.75	01100011	13.95	10100011	17.15	11100011	18.00
00100100	10.80	01100100	14.00	10100100	17.20	11100100	18.00
00100101	10.85	01100101	14.05	10100101	17.25	11100101	18.00
00100110	10.90	01100110	14.10	10100110	17.30	11100110	18.00
00100111	10.95	01100111	14.15	10100111	17.35	11100111	18.00
00101000	11.00	01101000	14.20	10101000	17.40	11101000	18.00
00101001	11.05	01101001	14.25	10101001	17.45	11101001	18.00
00101010	11.10	01101010	14.30	10101010	17.50	11101010	18.00
00101011	11.15	01101011	14.35	10101011	17.55	11101011	18.00
00101100	11.20	01101100	14.40	10101100	17.60	11101100	18.00
00101101	11.25	01101101	14.45	10101101	17.65	11101101	18.00
00101110	11.30	01101110	14.50	10101110	17.70	11101110	18.00
00101111	11.35	01101111	14.55	10101111	17.75	11101111	18.00
00110000	11.40	01110000	14.60	10110000	17.80	11110000	18.00
00110001	11.45	01110001	14.65	10110001	17.85	11110001	18.00
00110010	11.50	01110010	14.70	10110010	17.90	11110010	18.00
00110011	11.55	01110011	14.75	10110011	17.95	11110011	18.00
00110100	11.60	01110100	14.80	10110100	18.00	11110100	18.00
00110101	11.65	01110101	14.85	10110101	18.00	11110101	18.00
00110110	11.70	01110110	14.90	10110110	18.00	11110110	18.00
00110111	11.75	01110111	14.95	10110111	18.00	11110111	18.00
00111000	11.80	01111000	15.00	10111000	18.00	11111000	18.00
00111001	11.85	01111001	15.05	10111001	18.00	11111001	18.00
00111010	11.90	01111010	15.10	10111010	18.00	11111010	18.00
00111011	11.95	01111011	15.15	10111011	18.00	11111011	18.00
00111100	12.00	01111100	15.20	10111100	18.00	11111100	18.00
00111101	12.05	01111101	15.25	10111101	18.00	11111101	18.00
00111110	12.10	01111110	15.30	10111110	18.00	11111110	18.00
00111111	12.15	01111111	15.35	10111111	18.00	11111111	18.00

A.11 Junction temperature measure

Table 58. **TJ8 – Device Junction Temperature 8 bit reference version A, B and F**

Code	TJ (°C)	Code	TJ (°C)	Code	TJ (°C)	Code	TJ (°C)
00000000	TJ < -38	01000000	> 200	10000000	> 200	11000000	> 200
00000001	-38 < TJ < -34	01000001	> 200	10000001	> 200	11000001	> 200
00000010	-34 < TJ < -30	01000010	> 200	10000010	> 200	11000010	> 200

Code	TJ (°C)	Code	TJ (°C)	Code	TJ (°C)	Code	TJ (°C)
00000011	-30 < TJ < -26	01000011	> 200	10000011	> 200	11000011	> 200
00000100	-26 < TJ < -22	01000100	> 200	10000100	> 200	11000100	> 200
00000101	-22 < TJ < -18	01000101	> 200	10000101	> 200	11000101	> 200
00000110	-18 < TJ < -14	01000110	> 200	10000110	> 200	11000110	> 200
00000111	-14 < TJ < -10	01000111	> 200	10000111	> 200	11000111	> 200
00001000	-10 < TJ < -6	01001000	> 200	10001000	> 200	11001000	> 200
00001001	-6 < TJ < -2	01001001	> 200	10001001	> 200	11001001	> 200
00001010	-2 < TJ < 2	01001010	> 200	10001010	> 200	11001010	> 200
00001011	2 < TJ < 6	01001011	> 200	10001011	> 200	11001011	> 200
00001100	6 < TJ < 10	01001100	> 200	10001100	> 200	11001100	> 200
00001101	10 < TJ < 14	01001101	> 200	10001101	> 200	11001101	> 200
00001110	14 < TJ < 18	01001110	> 200	10001110	> 200	11001110	> 200
00001111	18 < TJ < 22	01001111	> 200	10001111	> 200	11001111	> 200
00010000	22 < TJ < 26	01010000	> 200	10010000	> 200	11010000	> 200
00010001	26 < TJ < 30	01010001	> 200	10010001	> 200	11010001	> 200
00010010	30 < TJ < 34	01010010	> 200	10010010	> 200	11010010	> 200
00010011	34 < TJ < 38	01010011	> 200	10010011	> 200	11010011	> 200
00010100	38 < TJ < 42	01010100	> 200	10010100	> 200	11010100	> 200
00010101	42 < TJ < 46	01010101	> 200	10010101	> 200	11010101	> 200
00010110	46 < TJ < 50	01010110	> 200	10010110	> 200	11010110	> 200
00010111	50 < TJ < 54	01010111	> 200	10010111	> 200	11010111	> 200
00011000	54 < TJ < 58	01011000	> 200	10011000	> 200	11011000	> 200
00011001	58 < TJ < 62	01011001	> 200	10011001	> 200	11011001	> 200
00011010	62 < TJ < 66	01011010	> 200	10011010	> 200	11011010	> 200
00011011	66 < TJ < 70	01011011	> 200	10011011	> 200	11011011	> 200
00011100	70 < TJ < 74	01011100	> 200	10011100	> 200	11011100	> 200
00011101	74 < TJ < 78	01011101	> 200	10011101	> 200	11011101	> 200
00011110	78 < TJ < 82	01011110	> 200	10011110	> 200	11011110	> 200
00011111	82 < TJ < 86	01011111	> 200	10011111	> 200	11011111	> 200
00100000	86 < TJ < 90	01100000	> 200	10100000	> 200	11100000	> 200
00100001	90 < TJ < 94	01100001	> 200	10100001	> 200	11100001	> 200
00100010	94 < TJ < 98	01100010	> 200	10100010	> 200	11100010	> 200
00100011	98 < TJ < 102	01100011	> 200	10100011	> 200	11100011	> 200
00100100	102 < TJ < 106	01100100	> 200	10100100	> 200	11100100	> 200
00100101	106 < TJ < 110	01100101	> 200	10100101	> 200	11100101	> 200
00100110	110 < TJ < 114	01100110	> 200	10100110	> 200	11100110	> 200
00100111	114 < TJ < 118	01100111	> 200	10100111	> 200	11100111	> 200
00101000	118 < TJ < 122	01101000	> 200	10101000	> 200	11101000	> 200
00101001	122 < TJ < 126	01101001	> 200	10101001	> 200	11101001	> 200
00101010	126 < TJ < 130	01101010	> 200	10101010	> 200	11101010	> 200
00101011	130 < TJ < 134	01101011	> 200	10101011	> 200	11101011	> 200

Code	TJ (°C)	Code	TJ (°C)	Code	TJ (°C)	Code	TJ (°C)
00101100	134 < TJ < 138	01101100	> 200	10101100	> 200	11101100	> 200
00101101	138 < TJ < 142	01101101	> 200	10101101	> 200	11101101	> 200
00101110	142 < TJ < 146	01101110	> 200	10101110	> 200	11101110	> 200
00101111	146 < TJ < 150	01101111	> 200	10101111	> 200	11101111	> 200
00110000	150 < TJ < 154	01110000	> 200	10110000	> 200	11110000	> 200
00110001	154 < TJ < 158	01110001	> 200	10110001	> 200	11110001	> 200
00110010	158 < TJ < 162	01110010	> 200	10110010	> 200	11110010	>200
00110011	162 < TJ <166	01110011	> 200	10110011	> 200	11110011	> 200
00110100	166 < TJ <170	01110100	> 200	10110100	> 200	11110100	> 200
00110101	170 < TJ <174	01110101	> 200	10110101	> 200	11110101	> 200
00110110	174 < TJ <178	01110110	> 200	10110110	> 200	11110110	> 200
00110111	178 < TJ <182	01110111	> 200	10110111	> 200	11110111	> 200
00111000	182 < TJ <186	01111000	> 200	10111000	> 200	11111000	> 200
00111001	186 < TJ <190	01111001	> 200	10111001	> 200	11111001	> 200
00111010	190 < TJ <194	01111010	> 200	10111010	> 200	11111010	> 200
00111011	194 < TJ <198	01111011	> 200	10111011	> 200	11111011	> 200
00111100	198 < TJ <200	01111100	> 200	10111100	> 200	11111100	> 200
00111101	>200	01111101	> 200	10111101	> 200	11111101	> 200
00111110	>200	01111110	> 200	10111110	> 200	11111110	> 200
00111111	>200	01111111	> 200	10111111	> 200	11111111	> 200

Table 59. Device Junction Temperature 8 bit reference version C and E

Code	TJ (°C)	Code	TJ (°C)	Code	TJ (°C)	Code	TJ (°C)
00000000	<-40	01000000	24	10000000	88	11000000	152
00000001	-39	01000001	25	10000001	89	11000001	153
00000010	-38	01000010	26	10000010	90	11000010	154
00000011	-37	01000011	27	10000011	91	11000011	155
00000100	-36	01000100	28	10000100	92	11000100	156
00000101	-35	01000101	29	10000101	93	11000101	157
00000110	-34	01000110	30	10000110	94	11000110	158
00000111	-33	01000111	31	10000111	95	11000111	159
00001000	-32	01001000	32	10001000	96	11001000	160
00001001	-31	01001001	33	10001001	97	11001001	161
00001010	-30	01001010	34	10001010	98	11001010	162
00001011	-29	01001011	35	10001011	99	11001011	163
00001100	-28	01001100	36	10001100	100	11001100	164
00001101	-27	01001101	37	10001101	101	11001101	165
00001110	-26	01001110	38	10001110	102	11001110	166
00001111	-25	01001111	39	10001111	103	11001111	167
00010000	-24	01010000	40	10010000	104	11010000	168

Code	TJ (°C)	Code	TJ (°C)	Code	TJ (°C)	Code	TJ (°C)
00010001	-23	01010001	41	10010001	105	11010001	169
00010010	-22	01010010	42	10010010	106	11010010	170
00010011	-21	01010011	43	10010011	107	11010011	171
00010100	-20	01010100	44	10010100	108	11010100	172
00010101	-19	01010101	45	10010101	109	11010101	173
00010110	-18	01010110	46	10010110	110	11010110	174
00010111	-17	01010111	47	10010111	111	11010111	175
00011000	-16	01011000	48	10011000	112	11011000	176
00011001	-15	01011001	49	10011001	113	11011001	177
00011010	-14	01011010	50	10011010	114	11011010	178
00011011	-13	01011011	51	10011011	115	11011011	179
00011100	-12	01011100	52	10011100	116	11011100	180
00011101	-11	01011101	53	10011101	117	11011101	181
00011110	-10	01011110	54	10011110	118	11011110	182
00011111	-9	01011111	55	10011111	119	11011111	183
00100000	-8	01100000	56	10100000	120	11100000	184
00100001	-7	01100001	57	10100001	121	11100001	185
00100010	-6	01100010	58	10100010	122	11100010	186
00100011	-5	01100011	59	10100011	123	11100011	187
00100100	-4	01100100	60	10100100	124	11100100	188
00100101	-3	01100101	61	10100101	125	11100101	189
00100110	-2	01100110	62	10100110	126	11100110	190
00100111	-1	01100111	63	10100111	127	11100111	191
00101000	0	01101000	64	10101000	128	11101000	192
00101001	1	01101001	65	10101001	129	11101001	193
00101010	2	01101010	66	10101010	130	11101010	194
00101011	3	01101011	67	10101011	131	11101011	195
00101100	4	01101100	68	10101100	132	11101100	196
00101101	5	01101101	69	10101101	133	11101101	197
00101110	6	01101110	70	10101110	134	11101110	198
00101111	7	01101111	71	10101111	135	11101111	199
00110000	8	01110000	72	10110000	136	11110000	200
00110001	9	01110001	73	10110001	137	11110001	> 200
00110010	10	01110010	74	10110010	138	11110010	> 200
00110011	11	01110011	75	10110011	139	11110011	> 200
00110100	12	01110100	76	10110100	140	11110100	> 200
00110101	13	01110101	77	10110101	141	11110101	> 200
00110110	14	01110110	78	10110110	142	11110110	> 200
00110111	15	01110111	79	10110111	143	11110111	> 200
00111000	16	01111000	80	10111000	144	11111000	>200
00111001	17	01111001	81	10111001	145	11111001	> 200

Code	TJ (°C)	Code	TJ (°C)	Code	TJ (°C)	Code	TJ (°C)
00111010	18	01111010	82	10111010	146	11111010	> 200
00111011	19	01111011	83	10111011	147	11111011	> 200
00111100	20	01111100	84	10111100	148	11111100	> 200
00111101	21	01111101	85	10111101	149	11111101	> 200
00111110	22	01111110	86	10111110	150	11111110	> 200
00111111	23	01111111	87	10111111	151	11111111	> 200

Table 60. TJ6 – Device Junction Temperature 6 bit reference version D

Code	TJ (°C)	Code	TJ (°C)	Code	TJ (°C)	Code	TJ (°C)
000000	-40	010000	16	100000	72	110000	128
000001	-36.5	010001	19.5	100001	75.5	110001	131.5
000010	-33	010010	23	100010	79	110010	135
000011	-29.5	010011	26.5	100011	82.5	110011	138.5
000100	-26	010100	30	100100	86	110100	142
000101	-22.5	010101	33.5	100101	89.5	110101	145.5
000110	-19	010110	37	100110	93	110110	149
000111	-15.5	010111	40.5	100111	96.5	110111	152.5
001000	-12	011000	44	101000	100	111000	156
001001	-8.5	011001	47.5	101001	103.5	111001	159.5
001010	-5	011010	51	101010	107	111010	163
001011	-1.5	011011	54.5	101011	110.5	111011	166.5
001100	2	011100	58	101100	114	111100	170
001101	5.5	011101	61.5	101101	117.5	111101	173.5
001110	9	011110	65	101110	121	111110	177
001111	12.5	011111	68.5	101111	124.5	111111	≥180.5

A.12 Set point voltage

Table 61. VSPFBK8 – Vsetpoint feedback 8 bit reference version A

Code	VSET (V)	Code	VSET (V)	Code	VSET (V)	Code	VSET (V)
00000000	10.6	01000000		10000000		11000000	
00000001	10.7	01000001		10000001		11000001	
00000010	10.8	01000010		10000010		11000010	
00000011	10.9	01000011		10000011		11000011	
00000100	11	01000100		10000100		11000100	
00000101	11.1	01000101		10000101		11000101	
00000110	11.2	01000110		10000110		11000110	
00000111	11.3	01000111		10000111		11000111	
00001000	11.4	01001000		10001000		11001000	
00001001	11.5	01001001		10001001		11001001	

Code	VSET (V)	Code	VSET (V)	Code	VSET (V)	Code	VSET (V)
00001010	11.6	01001010		10001010		11001010	
00001011	11.7	01001011		10001011		11001011	
00001100	11.8	01001100		10001100		11001100	
00001101	11.9	01001101		10001101		11001101	
00001110	12	01001110		10001110		11001110	
00001111	12.1	01001111		10001111		11001111	
00010000	12.2	01010000		10010000		11010000	
00010001	12.3	01010001		10010001		11010001	
00010010	12.4	01010010		10010010		11010010	
00010011	12.5	01010011		10010011		11010011	
00010100	12.6	01010100		10010100		11010100	
00010101	12.7	01010101		10010101		11010101	
00010110	12.8	01010110		10010110		11010110	
00010111	12.9	01010111		10010111		11010111	
00011000	13	01011000		10011000		11011000	
00011001	13.1	01011001		10011001		11011001	
00011010	13.2	01011010		10011010		11011010	
00011011	13.3	01011011		10011011		11011011	
00011100	13.4	01011100		10011100		11011100	
00011101	13.5	01011101		10011101		11011101	
00011110	13.6	01011110		10011110		11011110	
00011111	13.7	01011111		10011111		11011111	
00100000	13.8	01100000		10100000		11100000	
00100001	13.9	01100001		10100001		11100001	
00100010	14	01100010		10100010		11100010	
00100011	14.1	01100011		10100011		11100011	
00100100	14.2	01100100		10100100		11100100	
00100101	14.3	01100101		10100101		11100101	
00100110	14.4	01100110		10100110		11100110	
00100111	14.5	01100111		10100111		11100111	
00101000	14.6	01101000		10101000		11101000	
00101001	14.7	01101001		10101001		11101001	
00101010	14.8	01101010		10101010		11101010	
00101011	14.9	01101011		10101011		11101011	
00101100	15	01101100		10101100		11101100	
00101101	15.1	01101101		10101101		11101101	
00101110	15.2	01101110		10101110		11101110	
00101111	15.3	01101111		10101111		11101111	
00110000	15.4	01110000		10110000		11110000	
00110001	15.5	01110001		10110001		11110001	
00110010	15.6	01110010		10110010		11110010	

Code	VSET (V)	Code	VSET (V)	Code	VSET (V)	Code	VSET (V)
00110011	15.7	01110011		10110011		11110011	
00110100	15.8	01110100		10110100		11110100	
00110101	15.9	01110101		10110101		11110101	
00110110	16	01110110		10110110		11110110	
00110111	16	01110111		10110111		11110111	
00111000	16	01111000		10111000		11111000	
00111001	16	01111001		10111001		11111001	
00111010	16	01111010		10111010		11111010	
00111011	16	01111011		10111011		11111011	
00111100	16	01111100		10111100		11111100	
00111101	16	01111101		10111101		11111101	
00111110	16	01111110		10111110		11111110	
00111111	16	01111111		10111111		11111111	

Table 62. VSPFBK8B – Vsetpoint feedback 8 bit reference version B

Code	VSET (V)	Code	VSET (V)	Code	VSET (V)	Code	VSET (V)
00000000	10.6	01000000	12.2	10000000	13.8	11000000	15.4
00000001	10.625	01000001	12.225	10000001	13.825	11000001	15.425
00000010	10.65	01000010	12.25	10000010	13.85	11000010	15.45
00000011	10.675	01000011	12.275	10000011	13.875	11000011	15.475
00000100	10.7	01000100	12.3	10000100	13.9	11000100	15.5
00000101	10.725	01000101	12.325	10000101	13.925	11000101	15.525
00000110	10.75	01000110	12.35	10000110	13.95	11000110	15.55
00000111	10.775	01000111	12.375	10000111	13.975	11000111	15.575
00001000	10.8	01001000	12.4	10001000	14	11001000	15.6
00001001	10.825	01001001	12.425	10001001	14.025	11001001	15.625
00001010	10.85	01001010	12.45	10001010	14.05	11001010	15.65
00001011	10.875	01001011	12.475	10001011	14.075	11001011	15.675
00001100	10.9	01001100	12.5	10001100	14.1	11001100	15.7
00001101	10.925	01001101	12.525	10001101	14.125	11001101	15.725
00001110	10.95	01001110	12.55	10001110	14.15	11001110	15.75
00001111	10.975	01001111	12.575	10001111	14.175	11001111	15.775
00010000	11	01010000	12.6	10010000	14.2	11010000	15.8
00010001	11.025	01010001	12.625	10010001	14.225	11010001	15.825
00010010	11.05	01010010	12.65	10010010	14.25	11010010	15.85
00010011	11.075	01010011	12.675	10010011	14.275	11010011	15.875
00010100	11.1	01010100	12.7	10010100	14.3	11010100	15.9
00010101	11.125	01010101	12.725	10010101	14.325	11010101	15.925
00010110	11.15	01010110	12.75	10010110	14.35	11010110	15.95
00010111	11.175	01010111	12.775	10010111	14.375	11010111	15.975

Code	VSET (V)	Code	VSET (V)	Code	VSET (V)	Code	VSET (V)
00011000	11.2	01011000	12.8	10011000	14.4	11011000	16
00011001	11.225	01011001	12.825	10011001	14.425	11011001	16
00011010	11.25	01011010	12.85	10011010	14.45	11011010	16
00011011	11.275	01011011	12.875	10011011	14.475	11011011	16
00011100	11.3	01011100	12.9	10011100	14.5	11011100	16
00011101	11.325	01011101	12.925	10011101	14.525	11011101	16
00011110	11.35	01011110	12.95	10011110	14.55	11011110	16
00011111	11.375	01011111	12.975	10011111	14.575	11011111	16
00100000	11.4	01100000	13	10100000	14.6	11100000	16
00100001	11.425	01100001	13.025	10100001	14.625	11100001	16
00100010	11.45	01100010	13.05	10100010	14.65	11100010	16
00100011	11.475	01100011	13.075	10100011	14.675	11100011	16
00100100	11.5	01100100	13.1	10100100	14.7	11100100	16
00100101	11.525	01100101	13.125	10100101	14.725	11100101	16
00100110	11.55	01100110	13.15	10100110	14.75	11100110	16
00100111	11.575	01100111	13.175	10100111	14.775	11100111	16
00101000	11.6	01101000	13.2	10101000	14.8	11101000	16
00101001	11.625	01101001	13.225	10101001	14.825	11101001	16
00101010	11.65	01101010	13.25	10101010	14.85	11101010	16
00101011	11.675	01101011	13.275	10101011	14.875	11101011	16
00101100	11.7	01101100	13.3	10101100	14.9	11101100	16
00101101	11.725	01101101	13.325	10101101	14.925	11101101	16
00101110	11.75	01101110	13.35	10101110	14.95	11101110	16
00101111	11.775	01101111	13.375	10101111	14.975	11101111	16
00110000	11.8	01110000	13.4	10110000	15	11110000	16
00110001	11.825	01110001	13.425	10110001	15.025	11110001	16
00110010	11.85	01110010	13.45	10110010	15.05	11110010	16
00110011	11.875	01110011	13.475	10110011	15.075	11110011	16
00110100	11.9	01110100	13.5	10110100	15.1	11110100	16
00110101	11.925	01110101	13.525	10110101	15.125	11110101	16
00110110	11.95	01110110	13.55	10110110	15.15	11110110	16
00110111	11.975	01110111	13.575	10110111	15.175	11110111	16
00111000	12	01111000	13.6	10111000	15.2	11111000	16
00111001	12.025	01111001	13.625	10111001	15.225	11111001	16
00111010	12.05	01111010	13.65	10111010	15.25	11111010	16
00111011	12.075	01111011	13.675	10111011	15.275	11111011	16
00111100	12.1	01111100	13.7	10111100	15.3	11111100	16
00111101	12.125	01111101	13.725	10111101	15.325	11111101	16
00111110	12.15	01111110	13.75	10111110	15.35	11111110	16
00111111	12.175	01111111	13.775	10111111	15.375	11111111	16

A.13 Alternator speed measure

Table 63. **RPM8 – Alternator speed measure 8 bit reference version A and B**

Code	RPM	Code	RPM	Code	RPM	Code	RPM
00000000	n < 567	01000000	754	10000000	1134	11000000	2286
00000001	567	01000001	758	10000001	1143	11000001	2323
00000010	569	01000010	762	10000010	1152	11000010	2361
00000011	571	01000011	766	10000011	1161	11000011	2400
00000100	574	01000100	770	10000100	1171	11000100	2441
00000101	576	01000101	774	10000101	1180	11000101	2483
00000110	578	01000110	778	10000110	1190	11000110	2526
00000111	581	01000111	783	10000111	1200	11000111	2571
00001000	583	01001000	787	10001000	1210	11001000	2618
00001001	585	01001001	791	10001001	1220	11001001	2667
00001010	588	01001010	796	10001010	1231	11001010	2717
00001011	590	01001011	800	10001011	1241	11001011	2769
00001100	593	01001100	804	10001100	1252	11001100	2824
00001101	595	01001101	809	10001101	1263	11001101	2880
00001110	598	01001110	814	10001110	1274	11001110	2939
00001111	600	01001111	818	10001111	1286	11001111	3000
00010000	603	01010000	823	10010000	1297	11010000	3064
00010001	605	01010001	828	10010001	1309	11010001	3130
00010010	608	01010010	832	10010010	1321	11010010	3200
00010011	610	01010011	837	10010011	1333	11010011	3273
00010100	613	01010100	842	10010100	1346	11010100	3349
00010101	615	01010101	847	10010101	1358	11010101	3429
00010110	618	01010110	852	10010110	1371	11010110	3512
00010111	621	01010111	857	10010111	1385	11010111	3600
00011000	623	01011000	862	10011000	1398	11011000	3692
00011001	626	01011001	867	10011001	1412	11011001	3789
00011010	629	01011010	873	10011010	1426	11011010	3892
00011011	632	01011011	878	10011011	1440	11011011	4000
00011100	634	01011100	883	10011100	1455	11011100	4114
00011101	637	01011101	889	10011101	1469	11011101	4235
00011110	640	01011110	894	10011110	1485	11011110	4364
00011111	643	01011111	900	10011111	1500	11011111	4500
00100000	646	01100000	906	10100000	1516	11100000	4645
00100001	649	01100001	911	10100001	1532	11100001	4800
00100010	652	01100010	917	10100010	1548	11100010	4966
00100011	655	01100011	923	10100011	1565	11100011	5143
00100100	658	01100100	929	10100100	1582	11100100	5333

Code	RPM	Code	RPM	Code	RPM	Code	RPM
00100101	661	01100101	935	10100101	1600	11100101	5538
00100110	664	01100110	941	10100110	1618	11100110	5760
00100111	667	01100111	947	10100111	1636	11100111	6000
00101000	670	01101000	954	10101000	1655	11101000	6261
00101001	673	01101001	960	10101001	1674	11101001	6545
00101010	676	01101010	966	10101010	1694	11101010	6857
00101011	679	01101011	973	10101011	1714	11101011	7200
00101100	682	01101100	980	10101100	1735	11101100	7579
00101101	686	01101101	986	10101101	1756	11101101	8000
00101110	689	01101110	993	10101110	1778	11101110	8471
00101111	692	01101111	1000	10101111	1800	11101111	9000
00110000	696	01110000	1007	10110000	1823	11110000	9600
00110001	699	01110001	1014	10110001	1846	11110001	10286
00110010	702	01110010	1021	10110010	1870	11110010	11077
00110011	706	01110011	1029	10110011	1895	11110011	12000
00110100	709	01110100	1036	10110100	1920	11110100	13091
00110101	713	01110101	1043	10110101	1946	11110101	14400
00110110	716	01110110	1051	10110110	1973	11110110	16000
00110111	720	01110111	1059	10110111	2000	11110111	18000
00111000	724	01111000	1067	10111000	2028	11111000	20571
00111001	727	01111001	1075	10111001	2057	11111001	—
00111010	731	01111010	1083	10111010	2087	11111010	—
00111011	735	01111011	1091	10111011	2118	11111011	—
00111100	738	01111100	1099	10111100	2149	11111100	—
00111101	742	01111101	1108	10111101	2182	11111101	—
00111110	746	01111110	1116	10111110	2215	11111110	—
00111111	750	01111111	1125	10111111	2250	11111111	—

Revision history

Table 64. **Document revision history**

Date	Version	Changes
17-Jun-2019	1	Initial release.
08-Sep-2022	2	Document classification changed from Restricted to public.

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